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SD9613-170
12-bit, 170MHz, Dual Channel ADC

SD9613 OVERVIEW

The SD9613 is a dual-channel, 12-bit, analog-to-digital converter (ADC) supporting sampling rates up to 170MSps. The device uses a multistage pipeline architecture to achieve high signal-to-noise ratio (SNR) and linearity, over wide input signal bandwidth. The SD9613 uses a LVDS output interface to transfer the data out. Programming for configuration and control is accomplished using a 3-wire SPI-compatible serial bus. The digital output data can be programmed to be delivered in offset binary, twos complement format, or gray code.

FEATURES

- SNR: 70.8dBFS at f_{IN} = 70.2MHz and f_S = 170MSps
- SFDR: 88.0dBc at f_{IN} = 70.2MHz and f_S = 170MSps
- -151.3dBFS/Hz input-noise at f_{IN} = 70.2MHz and f_S = 170MSps
- $2.0V_{p\text{-}p}$ nominal input
- Typical power consumption: 495mW at 170MSps
- Integer 1-to-8 input clock divider (1000MHz maximum input rate)
- Sample rates of up to 170MSps
- 1.8V analog supply voltage
- LVDS (ANSI-644 levels) outputs
- Internal ADC voltage reference
- ADC clock duty cycle correction
- Serial port control
- Energy saving power-down modes

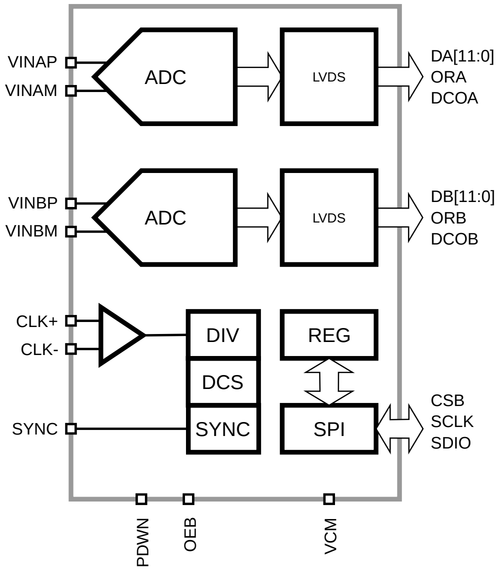

Figure 1: SD9613 Functional Block Diagram.

APPLICATIONS

- Communications
- General-purpose software radios
- I/Q demodulation systems
- Diversity radio systems
- Smart antenna systems
- Multimode digital receivers
- Ultrasound equipment
- Radar/LiDAR applications
- Broadband data applications

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SPECIFICATIONS

DC Specifications

At T_A = 25°C, V_{AVDD} = 1.8V, V_{DRVDD} = 1.8V, F_{CLK} = 170MHz, A_{IN} = -1dBFS, differential AC-coupled external clock source, LVDS mode, unless otherwise noted.

Table 1. DC Specifications.

PARAMETER		TEMP	MIN	TYP	MAX	UNIT
Resolution				12		bits
Accuracy						
	No Missing Codes	Full		Guaranteed		
	Offset Error	Full	-0.50		0.50	%FSR
	Gain Error	Full	-8.00		-1.00	%FSR
	DNL	Full			±0.5	LSB
	INL	Full			±0.8	LSB
Matching						
	Offset Error	25°C	-0.80		0.80	%FSR
	Gain Error	25°C	-0.50		0.50	%FSR
Temperature Drift						
	Offset Error	Full		+/-0.5		ppm/°C
	Gain Error	Full		80.0		ppm/°C
External Voltage Reference						
	Range	Full	0.90		1.07	V
Input Referred Noise						
	V_{REF} = 1.0V	25°C		0.36		LSB(rms)
Analog Input						
	Input Span, VREF = 1.04V	Full		2.0		V
	Input Capacitance	Full		6.0		pF
	Input Resistance	Full		2.0		kΩ
	Input Common-Mode Voltage	Full		0.70		V
	Input Common-Mode Range	Full	0.62		0.93	V
	VCM Voltage	Full		0.70		V
	VCM Current Capability	Full		100		µA
Reference Input Resistance		Full		50		kΩ
Power Supply						
	V_{AVDD}	Full	1.7	1.8	1.9	V
	V_{DRVDD}	Full	1.7	1.8	1.9	µA
	I_{AVDD} @1.8V	Full		224.0	285.0	mA
	I_{DRVDD} @1.8V	Full		56.0	65.0	mA
Power Consumption						
	Sine Wave Input	Full		495.0		mW
	Standby[1]	Full		60.0		mW
	Power Down	Full		8.0		mW

[1] Standby power is measured with a sinewave input and active clock.

AC Specifications

At T_A = 25°C, V_{AVDD} = 1.8V, V_{DRVDD} = 1.8V, F_{CLK} = 170MHz, A_{IN} = -1dBFS, differential AC-coupled external clock source, High-Performance Calibration Mode enabled, LVDS mode, unless otherwise noted.

Table 2. AC Specifications.

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
Signal-to-Noise Ratio (SNR)					
f_{IN} = 30.2MHz	25°C		71.0		dBFS
f_{IN} = 70.2MHz	25°C		70.8		dBFS
	Full	69.5			dBFS
f_{IN} = 140MHz	25°C		70.0		dBFS
f_{IN} = 220MHz	25°C		68.8		dBFS
Signal-to-Noise and Distortion Ratio (SNDR)					
f_{IN} = 30.2MHz	25°C		70.7		dBFS
f_{IN} = 70.2MHz	25°C		70.5		dBFS
	Full	68.5			dBFS
f_{IN} = 140MHz	25°C		69.4		dBFS
f_{IN} = 220MHz	25°C		67.9		dBFS
Effective Number of Bits (ENOB)					
f_{IN} = 30.2MHz	25°C		11.5		bits
f_{IN} = 70.2MHz	25°C		11.4		bits
f_{IN} = 140MHz	25°C		11.2		bits
f_{IN} = 220MHz	25°C		11.0		bits
Worst 2nd or 3rd Harmonic Power					
f_{IN} = 30.2MHz	25°C		-89.0		dBc
f_{IN} = 70.2MHz	25°C		-83.0	-81.0	dBc
f_{IN} = 140MHz	25°C		-82.0		dBc
f_{IN} = 220MHz	25°C		-77.0		dBc
Worst non-Harmonic Power					
f_{IN} = 30.2MHz	25°C		-89.0		dBc
f_{IN} = 70.2MHz	25°C		-83.0	-82.0	dBc
f_{IN} = 140MHz	25°C		-82.0		dBc
f_{IN} = 220MHz	25°C		-81.0		dBc
Spurious-Free Dynamic Range[1] (SFDR)					
f_{IN} = 30.2MHz	25°C		89.0		dBc
f_{IN} = 70.2MHz	25°C		88.0		dBc
	Full	80.0			dBc
f_{IN} = 140MHz	25°C		82.0		dBc
f_{IN} = 220MHz	25°C		77.0		dBc
Two-Tone SFDR					
f_{IN1} = 183.0MHz, f_{IN2} = 187.0MHz	25°C		86.6		dBc
Crosstalk[2]	25°C		-105.0		dBc
Analog Input Bandwidth	Full		650.0		MHz

[1] SFDR excludes the DC and $f_S/2$ bins.

[2] Crosstalk is measured at 100MHz with -1.0dBFS on one channel and no input on the alternate channel.

Digital Specification

V_{AVDD} = 1.8V, V_{DRVDD} = 1.8V, F_{CLK} = 170MHz, A_{IN} = -1dBFS, differential AC-coupled external clock source, DCS disabled, unless otherwise noted.

Table 3. Differential Clock Input.

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
Logic Compliance	Full		CMOS/LVDS/LVPECL		
Internal Common-Mode Bias	Full		0.9		V
Differential Input Voltage	Full	0.3		1.2	$V_{p\text{-}p}$
Input Voltage Range	Full	V_{AGND}-0.3		V_{AVDD}+0.2	V
Input Common-Mode Range	Full	0.75		1.05	V
High Level Input Current	Full	-10		10	µA
Low Level Input Current	Full	-10		10	µA
Input Capacitance	Full		1.7		pF
Input Resistance	Full		6.0		kΩ

Table 4. SYNC Input.

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
Logic Compliance	Full		CMOS		
Input Voltage Range	Full	V_{AGND}		V_{AVDD}	V
High Level Input Voltage	Full	1.22		V_{AVDD}	V
Low Level Input Voltage	Full	V_{AGND}		0.50	V
High Level Input Current	Full	-1		1	µA
Low Level Input Current	Full	-1		1	µA
Input Capacitance	Full		1.5		pF
Input Resistance	Full		100		kΩ

Table 5. CSB Input.

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
High Level Input Voltage	Full	1.22			V
Low Level Input Voltage	Full			0.6	V
High Level Input Current	Full	-1		1	µA
Low Level Input Current	Full	-1		1	µA
Input Capacitance	Full		1.5		pF
Input Resistance	Full		100		kΩ

Table 6. SCLK Input.

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
High Level Input Voltage	Full	1.22			V
Low Level Input Voltage	Full			0.6	V
High Level Input Current	Full	-1		1	µA
Low Level Input Current	Full	-1		1	µA
Input Capacitance	Full		1.5		pF
Input Resistance	Full		100		kΩ

Table 7. SDIO Input.

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
High Level Input Voltage	Full	1.22			V
Low Level Input Voltage	Full			0.6	V
High Level Input Current	Full	-1		1	µA
Low Level Input Current	Full	-1		1	µA
Input Capacitance	Full		1.5		pF
Input Resistance	Full		100		kΩ

Table 8. OEB Input.

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
High Level Input Voltage	Full	1.22			V
Low Level Input Voltage	Full			0.6	V
High Level Input Current	Full	-1		1	µA
Low Level Input Current	Full	-1		1	µA
Input Capacitance	Full		1.5		pF
Input Resistance	Full		100		kΩ

Table 9. PDWN Input.

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
High Level Input Voltage	Full	1.22			V
Low Level Input Voltage	Full			0.6	V
Pull-down Current @1.8V	Full			90	µA
Input Capacitance	Full		1.5		pF
Input Resistance	Full		28		kΩ

Table 10. LVDS Outputs (DATA and OR).

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
Differential Output Voltage (V_{OD}), ANSI Mode	Full	250	300	450	mV
Output Offset Voltage (V_{OS}), ANSI Mode	Full	1.10	1.13	1.30	V
Differential Output Voltage (V_{OD}), Reduced Swing	Full	150	220	285	mV
Output Offset Voltage (V_{OS}), Reduced Swing	Full	1.10	1.22	1.30	V

Switching Specifications

V_{AVDD} = 1.8V, V_{DRVDD} = 1.8V, F_{CLK} = 170MHz, A_{IN} = -1dBFS, differential AC-coupled sine wave external clock source, DCS enabled, unless otherwise noted.

Table 11. Clock Input Timing.

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
Input Clock Rate	Full			1000.0	MHz
Conversion Rate (after clock divider)	Full	20.0		170.0	MHz
CLK Pulse Width High (t_{CH})					
Divide-by-1 Mode, DCS Enabled	Full	1.5			ns
Divide-by-1 Mode, DCS Disabled	Full	2.8	3.0	3.1	ns
Divide-by-2 Mode Through Divide-by-8 Mode	Full	0.6			ns
Aperture Delay (t_A)	Full		0.5		ns
Aperture Uncertainty (Jitter, t_J)	Full		140.0		fs

Table 12. SYNC Timing Requirements.

PARAMETER	MIN	TYP	MAX	UNIT
Set-Up Time ($t_{S,SYNC}$)		0.35		ns
Hold Time ($t_{H,SYNC}$)		0.35		ns

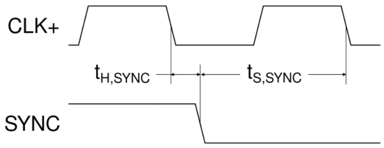


Figure 2: SYNC Input Timing.

Table 13. Data Output.

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
LVDS Mode					
Data Propagation Delay (t_{PD})	Full		8.0		ns
DCO Propagation Delay (t_{DCO})	Full		7.7		ns
DCO to Data Skew (t_{SKEW})	Full	-0.5	0.1	0.7	ns
Pipeline Delay (Latency, L) Channel A/Channel B	Full		32/32.5		Cycles
Wake-Up Time (from sleep)	Full		5.0		µs
Wake-Up Time (from power down)	Full		250.0		µs
Out-of-Range Recovery Time	Full		3		Cycles

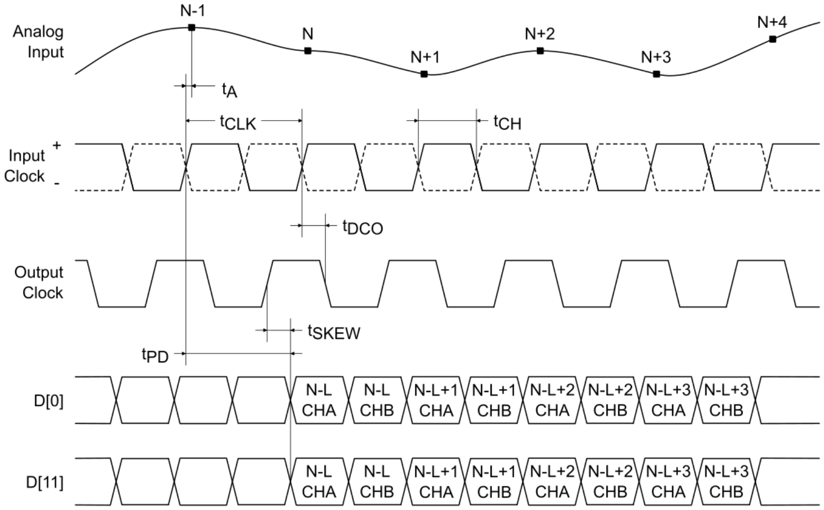


Figure 3: Parallel LVDS Output Mode Timing.

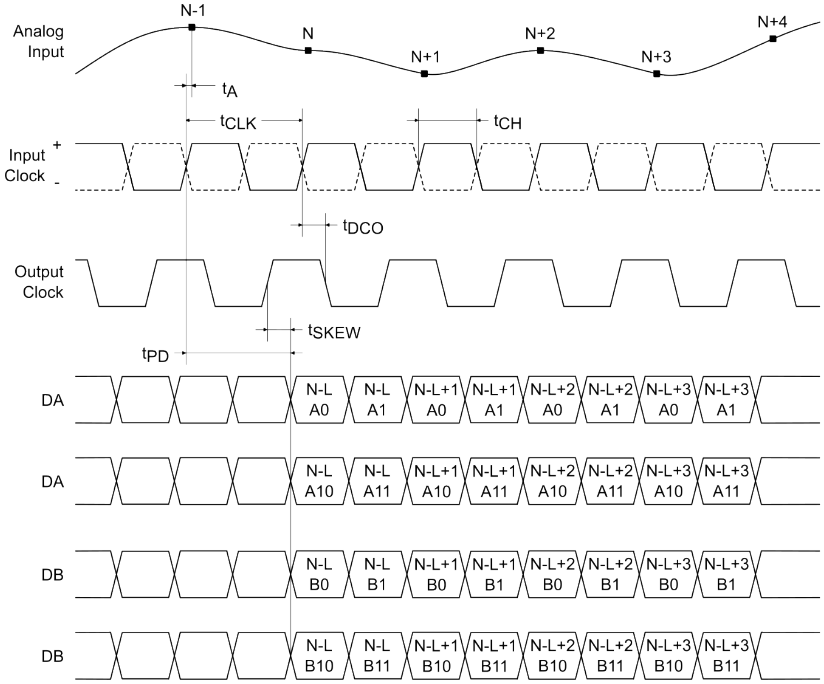


Figure 4: Channel Multiplexed LVDS Output Mode Timing.

Output Modes

Two LVDS samples are sent out every clock cycle using both the rising and the falling edge of the output clock. In interleaved parallel mode, the two ADCs share the full set of output pins. The first half-cycle contains ADC A data and the second ADC B data. In multiplexed mode, each ADC has its dedicated set of output pins and the data is sent out even numbered bits on the first half-cycle and the odd bits on the second. Register *0x465*, bits [2:0], control the interleaving/multiplexing.

Output Timing Control

Bits [13:10], in register *0x473*, control the output clock delay relative to output data, while bit [14] inverts the clock. The delay step size is about 250ps.

ABSOLUTE MAXIMUM RATINGS

Table 14. Absolute Maximum Ratings (T_A = 25°C, unless otherwise specified).

Parameter	Symbol	Conditions	Min	Max	Units
AVDD	V_{AVDD}	Relative to AGND	-0.3	2.0	V
DRVDD	V_{DRVDD}	Relative to AGND	-0.3	2.0	V
VINAP/VINBP, VINAM/VINBM		Relative to AGND	-0.3	2.0	V
CLK+, CLK-		Relative to AGND	-0.3	2.0	V
SYNC		Relative to AGND	-0.3	2.0	V
VCM		Relative to AGND	-0.3	2.0	V
CSB		Relative to AGND	-0.3	2.0	V
SCLK		Relative to AGND	-0.3	2.0	V
SDIO		Relative to AGND	-0.3	2.0	V
OEB		Relative to AGND	-0.3	2.0	V
PDWN		Relative to AGND	-0.3	2.0	V
D0+/-, ..., D11+/-		Relative to AGND	-0.3	2.0	V
DCO+, DCO-		Relative to AGND	-0.3	2.0	V
Operating Temperature Range (Ambient)			-40	85	°C
Maximum Junction Temperature Under Bias				125	
Storage Temperature Range (Ambient)			-65	150	

Notes:

1. Stresses beyond those listed under Table 14 may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

ESD CAUTION.

	**Electrostatic Discharge Sensitive Device.** Proper ESD precautions should be observed to prevent performance degradation or loss of functionality.

PACKAGE

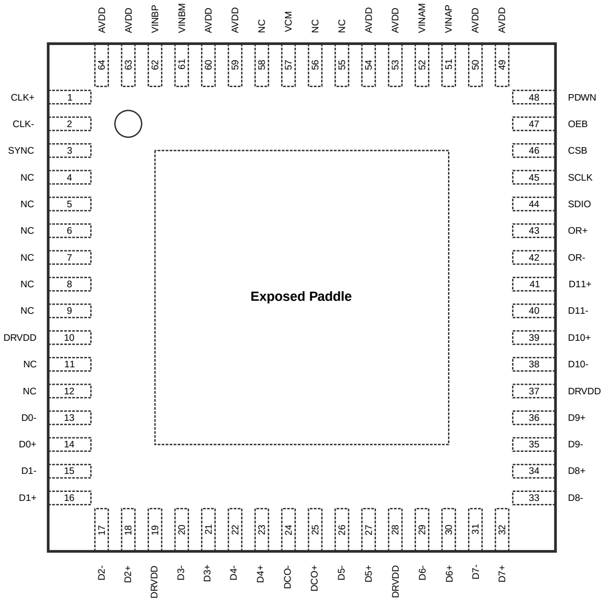


Figure 5: SD9613 Package Top View for Parallel LVDS Configuration.

1. NC = No Connect.
2. The exposed thermal pad on the bottom of the package provides the analog ground for the part and must be connected for proper operation.

Table 15. Pin Descriptions for Parallel LVDS Configuration.

Number	Name	Type	Comment
0	AGND	Ground	Exposed Paddle, Analog Ground.
1	CLK+	Input	ADC Clock Input (Plus).
2	CLK-	Input	ADC Clock Input (Minus).
3	SYNC	Input	Digital Synchronization Pin.
4, 5, 6, 7, 8, 9, 11, 12, 55, 56, 58	NC		Do not connect.
10, 19, 28, 37	DRVDD	Power	Digital I/O Supply.
13	D0-	Output	Channel A/Channel B LVDS Output Data 0 (Minus).
14	D0+	Output	Channel A/Channel B LVDS Output Data 0 (Plus).
15	D1-	Output	Channel A/Channel B LVDS Output Data 1 (Minus).
16	D1+	Output	Channel A/Channel B LVDS Output Data 1 (Plus).
17	D2-	Output	Channel A/Channel B LVDS Output Data 2 (Minus).
18	D2+	Output	Channel A/Channel B LVDS Output Data 2 (Plus).
20	D3-	Output	Channel A/Channel B LVDS Output Data 3 (Minus).
21	D3+	Output	Channel A/Channel B LVDS Output Data 3 (Plus).
22	D4-	Output	Channel A/Channel B LVDS Output Data 4 (Minus).
23	D4+	Output	Channel A/Channel B LVDS Output Data 4 (Plus).
24	DCO-	Output	LVDS Data Clock Output (Minus).
25	DCO+	Output	LVDS Data Clock Output (Plus).
26	D5-	Output	Channel A/Channel B LVDS Output Data 5 (Minus).

Number	Name	Type	Comment
27	D5+	Output	Channel A/Channel B LVDS Output Data 5 (Plus).
29	D6-	Output	Channel A/Channel B LVDS Output Data 6 (Minus).
30	D6+	Output	Channel A/Channel B LVDS Output Data 6 (Plus).
31	D7-	Output	Channel A/Channel B LVDS Output Data 7 (Minus).
32	D7+	Output	Channel A/Channel B LVDS Output Data 7 (Plus).
33	D8-	Output	Channel A/Channel B LVDS Output Data 8 (Minus).
34	D8+	Output	Channel A/Channel B LVDS Output Data 8 (Plus).
35	D9-	Output	Channel A/Channel B LVDS Output Data 9 (Minus).
36	D9+	Output	Channel A/Channel B LVDS Output Data 9 (Plus).
38	D10-	Output	Channel A/Channel B LVDS Output Data 10 (Minus).
39	D10+	Output	Channel A/Channel B LVDS Output Data 10 (Plus).
40	D11-	Output	Channel A/Channel B LVDS Output Data 11 (Minus).
41	D11+	Output	Channel A/Channel B LVDS Output Data 11 (Plus).
42	OR-	Output	Channel A/Channel B LVDS Overrange (Minus).
43	OR+	Output	Channel A/Channel B LVDS Overrange (Plus).
44	SDIO	InOut	SPI Serial Data I/O.
45	SCLK	Input	This pin functions as a serial interface clock input when RESET is low. It controls the low-speed mode when RESET is tied high. This pin has an internal pulldown resistor.
46	CSB	Input	SPI Chip Select (Active Low).
47	OEB	Input	Output Enable Input (Active low).
48	PDWN	Input	Power-Down Input (Active High). The operation of this pin depends on the SPI mode and can be configured as power-down or standby.
49, 50, 53, 54, 59, 60, 63, 64	AVDD	Power	Analog Power Supply (1.8 V Nominal).
51	VINAP	Input	Differential Analog Input Pin (Plus) for Channel A.
52	VINAM	Input	Differential Analog Input Pin (Minus) for Channel A.
57	VCM	Output	This pin outputs the common-mode voltage that can be used externally to bias the analog input pins.
61	VINBM	Input	Differential Analog Input Pin (Minus) for Channel B.
62	VINBP	Input	Differential Analog Input Pin (Plus) for Channel B.

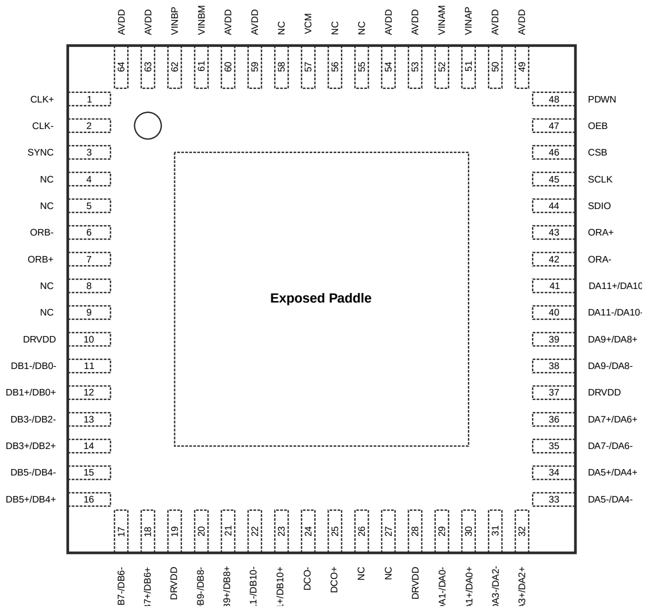


Figure 6: SD9613 Package Top View for Channel Multiplexed LVDS Configuration.

1. NC = No Connect.
2. The exposed thermal pad on the bottom of the package provides the analog ground for the part and must be connected for proper operation.

Table 16. Pin Descriptions for Channel Multiplexed LVDS Configuration.

Number	Name	Type	Comment
0	AGND	Ground	Exposed Paddle, Analog Ground.
1	CLK+	Input	ADC Clock Input (Plus).
2	CLK-	Input	ADC Clock Input (Minus).
3	SYNC	Input	Digital Synchronization Pin.
4, 5, 8, 9, 26, 27, 55, 56, 58	NC		Do not connect.
6	ORB-	Output	Channel B LVDS Overflow Output (Minus).
7	ORB+	Output	Channel B LVDS Overflow Output (Plus).
10, 19, 28, 37	DRVDD	Power	Digital I/O Supply.
11	DB1-/DB0-	Output	Channel B LVDS Output Data 0 and 1 (Minus).
12	DB1+/DB0+	Output	Channel B LVDS Output Data 0 and 1 (Plus).
13	DB3-/DB2-	Output	Channel B LVDS Output Data 2 and 3 (Minus).
14	DB3+/DB2+	Output	Channel B LVDS Output Data 2 and 3 (Plus).
15	DB5-/DB4-	Output	Channel B LVDS Output Data 4 and 5 (Minus).
16	DB5+/DB4+	Output	Channel B LVDS Output Data 4 and 5 (Plus).
17	DB7-/DB6-	Output	Channel B LVDS Output Data 6 and 7 (Minus).
18	DB7+/DB6+	Output	Channel B LVDS Output Data 6 and 7 (Plus).
20	DB9-/DB8-	Output	Channel B LVDS Output Data 8 and 9 (Minus).
21	DB9+/DB8+	Output	Channel B LVDS Output Data 8 and 9 (Plus).
22	DB11-/DB10-	Output	Channel B LVDS Output Data 10 and 11 (Minus).
23	DB11+/DB10+	Output	Channel B LVDS Output Data 10 and 11 (Plus).

Number	Name	Type	Comment
24	DCO-	Output	LVDS Data Clock Output (Minus).
25	DCO+	Output	LVDS Data Clock Output (Plus).
29	DA1-/DA0-	Output	Channel A LVDS Output Data 0 and 1 (Minus).
30	DA1+/DA0+	Output	Channel A LVDS Output Data 0 and 1 (Plus).
31	DA3-/DA2-	Output	Channel A LVDS Output Data 2 and 3 (Minus).
32	DA3+/DA2+	Output	Channel A LVDS Output Data 2 and 3 (Plus).
33	DA5-/DA4-	Output	Channel A LVDS Output Data 4 and 5 (Minus).
34	DA5+/DA4+	Output	Channel A LVDS Output Data 4 and 5 (Plus).
35	DA7-/DA6-	Output	Channel A LVDS Output Data 6 and 7 (Minus).
36	DA7+/DA6+	Output	Channel A LVDS Output Data 6 and 7 (Plus).
38	DA9-/DA8-	Output	Channel A LVDS Output Data 8 and 9 (Minus).
39	DA9+/DA8+	Output	Channel A LVDS Output Data 8 and 9 (Plus).
40	DA11-/DA10-	Output	Channel A LVDS Output Data 10 and 11 (Minus).
41	DA11+/DA10+	Output	Channel A LVDS Output Data 10 and 11 (Plus).
42	ORA-	Output	Channel A LVDS Overflow Output (Minus).
43	ORA+	Output	Channel A LVDS Overflow Output (Plus).
44	SDIO	InOut	SPI Serial Data I/O.
45	SCLK	Input	This pin functions as a serial interface clock input when RESET is low. It controls the low-speed mode when RESET is tied high. This pin has an internal pulldown resistor.
46	CSB	Input	SPI Chip Select (Active Low).
47	OEB	Input	Output Enable Input (Active low).
48	PDWN	Input	Power-Down Input (Active High). The operation of this pin depends on the SPI mode and can be configured as power-down or standby.
49, 50, 53, 54, 59, 60, 63, 64	AVDD	Power	Analog Power Supply (1.8 V Nominal).
51	VINAP	Input	Differential Analog Input Pin (Plus) for Channel A.
52	VINAM	Input	Differential Analog Input Pin (Minus) for Channel A.
57	VCM	Output	This pin outputs the common-mode voltage that can be used externally to bias the analog input pins.
61	VINBM	Input	Differential Analog Input Pin (Minus) for Channel B.
62	VINBP	Input	Differential Analog Input Pin (Plus) for Channel B.

TYPYCAL PERFORMANCE CHARACTERISTICS

At T_A = 25°C, V_{AVDD} = 1.8V, V_{DRVDD} = 1.8V, F_{CLK} = 170MHz, A_{IN} = -1dBFS, differential AC-coupled clock source, High-Performance Calibration Mode enabled, LVDS mode, unless otherwise noted.

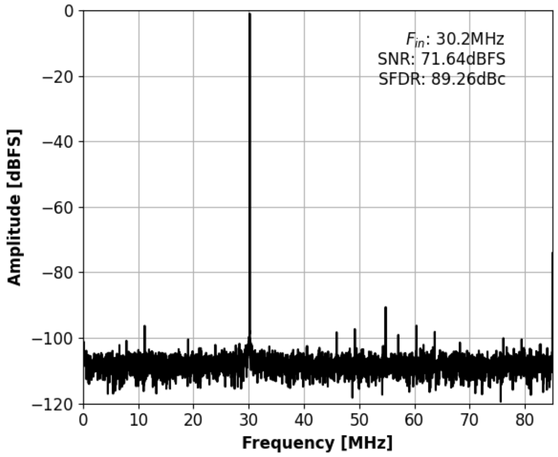


Figure 7: Single-Tone FFT with f_{IN}=30.2MHz.

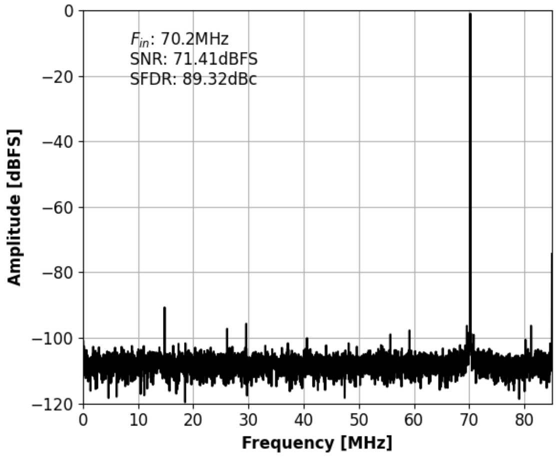


Figure 8: Single-Tone FFT with f_{IN}=70.2MHz.

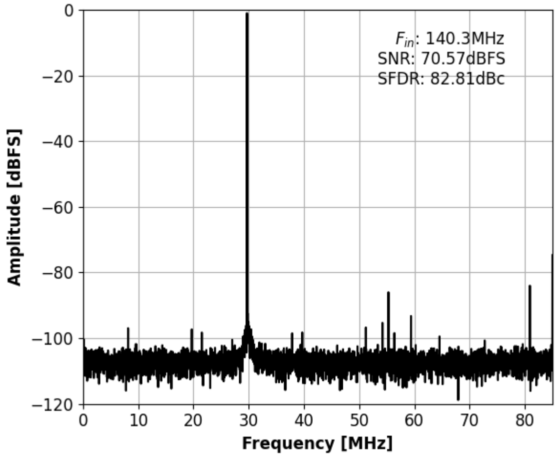


Figure 9: Single-Tone FFT with f_{IN}=140MHz.

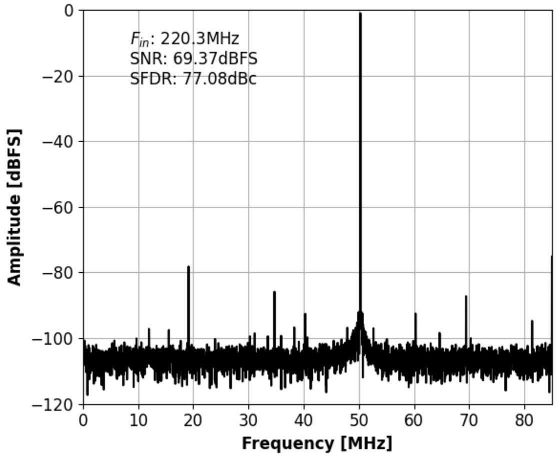


Figure 10: Single-Tone FFT with f_{IN}=220MHz.

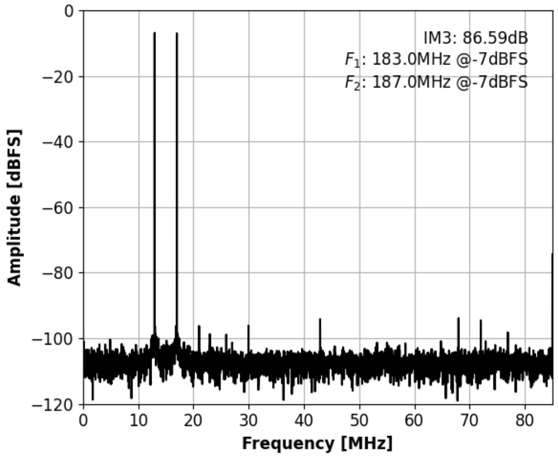


Figure 11: Two-Tone FFT with f_{IN1}=183.0MHz, f_{IN2}=187.0MHz.

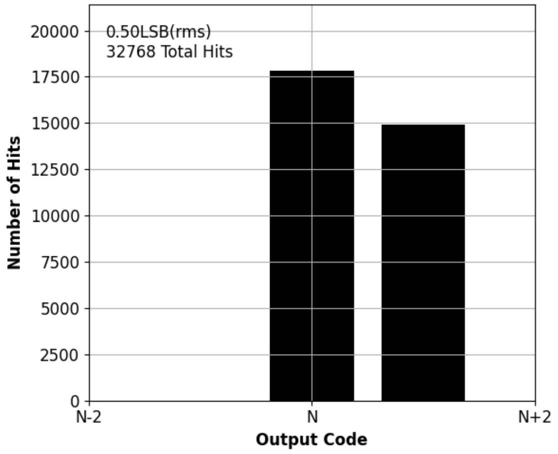
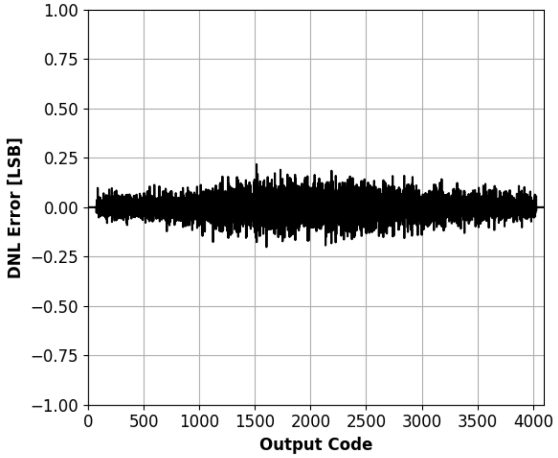


Figure 12: Grounded Input Histogram.



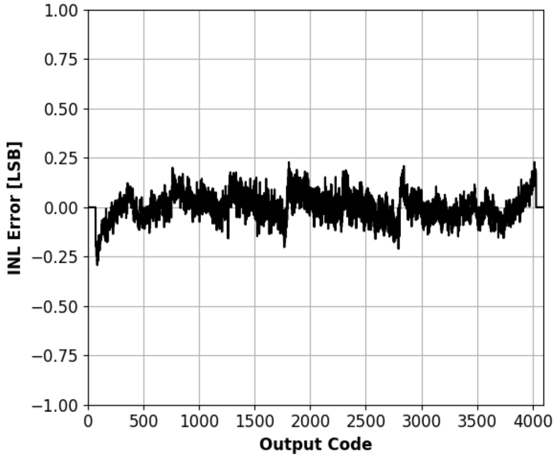
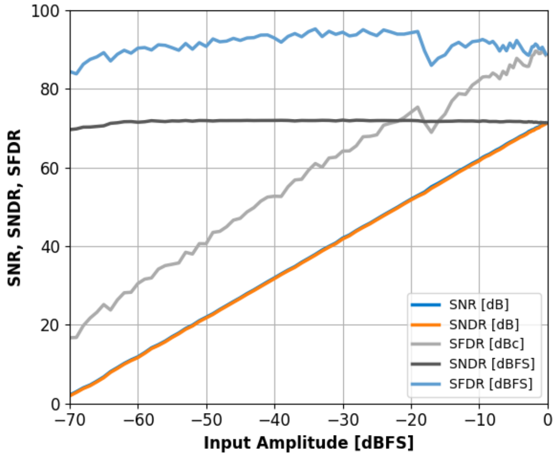


Figure 13: DNL Error with f_{IN}=6.55MHz.

Figure 14: INL Error with f_{IN}=6.55MHz.



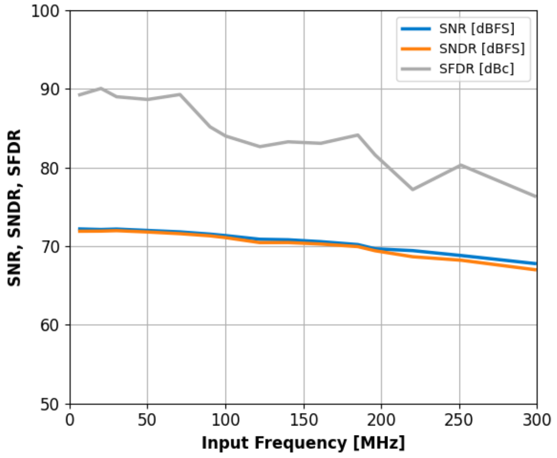
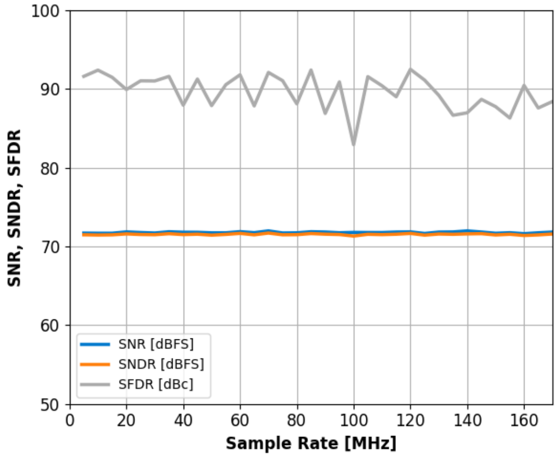


Figure 15: Single-Tone SNR, SNDR and SFDR vs. Input Amplitude with f_{IN}=70.25MHz.

Figure 16: Single-Tone SNR, SNDR and SFDR vs. Input Frequency with f_S=170MHz.



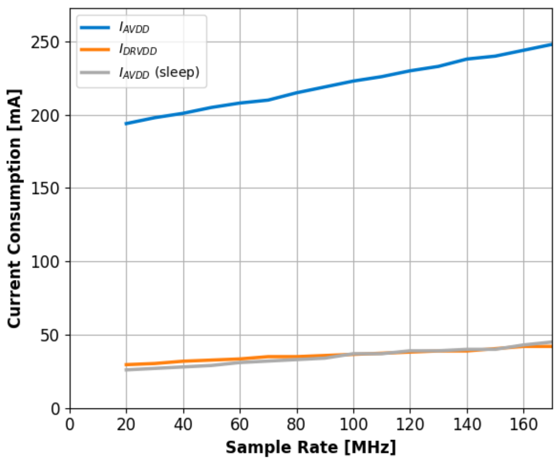


Figure 17: Single-Tone SNR, SNDR and SFDR vs. Sample Rate with f_{IN}=70.25MHz.

Figure 18: Current vs. Sample Rate.

EQUIVALENT CIRCUITS

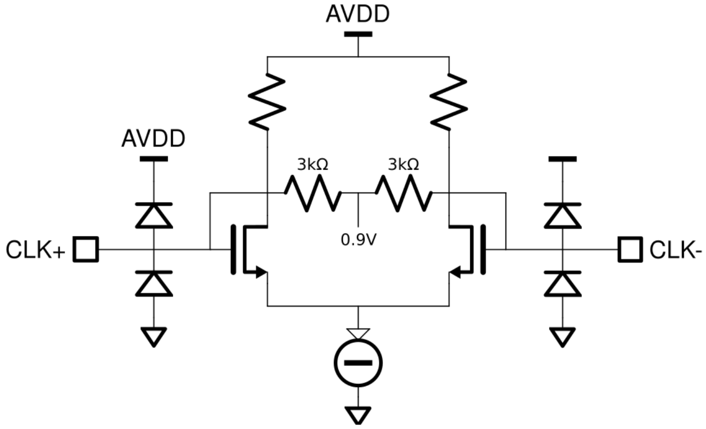


Figure 19: Equivalent Clock Input Circuit.

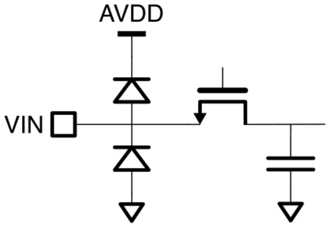


Figure 20: Equivalent Analog Input Circuit.

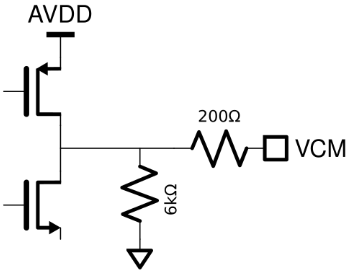


Figure 21: Equivalent VCM Circuit.

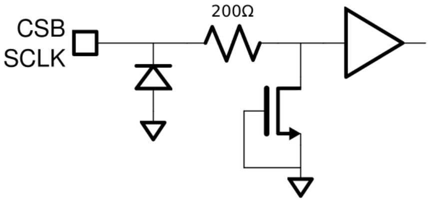


Figure 22: Equivalent CSB or SCLK Input Circuit.

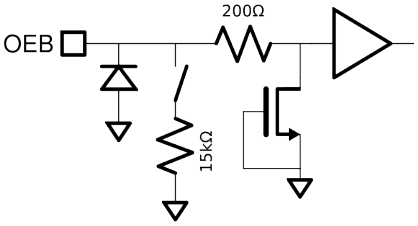


Figure 23: Equivalent OEB Input Circuit.

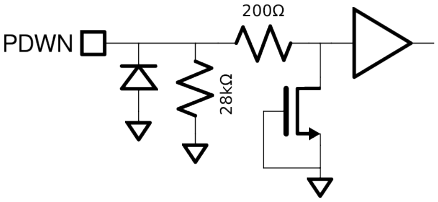


Figure 24: Equivalent PDWN Input Circuit.

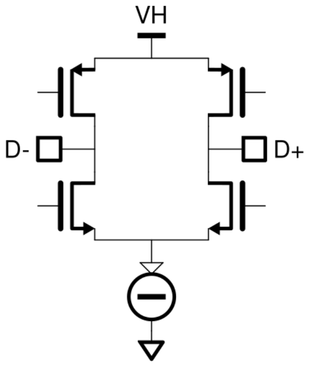


Figure 25: Equivalent LVDS output Circuit.

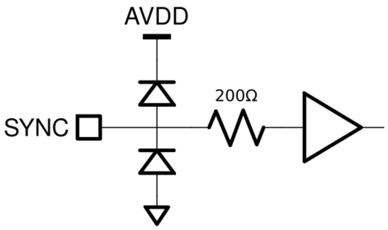


Figure 26: Equivalent SYNC Input Circuit.

THEORY OF OPERATION

ADC Architecture

The ADC uses a pipelined architecture and innovative patented switched-capacitor circuits. Its fully differential design provides exceptional immunity to power supply noise and minimizes reference voltage self-modulation. A built-in Sample-and-Hold (S/H) function is integrated into the input stage of the pipeline structure.

Analog Input

The input stage of the ADC behaves as a switched-capacitor network, presenting itself to the driving circuit as a combination of a switch and a sampling capacitor. The capacitor is reset prior to each conversion cycle, effectively eliminating non-linear memory effects commonly observed in some pipelined ADC architectures. The ADC does not include an internal common-mode bias therefore, the driving source must provide an appropiate common-mode voltage.

Differential Clock Input

The SD9613 features a differential clock receiver with an integrated common-mode bias. For proper operation, the clock inputs should be AC-coupled using 10nF capacitors.

Differential Clock Configuration. For optimal jitter performance, a differential clock source is recommended. The differential clock signals to CLK+ and CLK- should be connected through a 10nF AC-coupling capacitors.

Single-Ended Clock Configuration. If a single-ended clock source is used, the signal source should be AC-coupled to the CLK+ pin. In this configuration, a 10nF capacitor should be connected between the CLK- pin and analog ground to maintain proper biasing.

Clock Jitter Considerations. Clock jitter has a significant impact on the ADC's signal-to-noise ratio (SNR). The sensitivity to jitter increases with input signal frequency. For best performance, a low-noise differential clock with fast edge transitions should be used.

Note: In some conditions the part can enter in manufacturing test mode if both differential clock inputs are held low for more than 1ms. This behavior can be prevented by writing 1 to register *0x4cf*, bit[15].

Clock Divider

The ADC includes a programmable clock divider that allows the input clock to be divided by integer values from 2 to 8. The divider is configured by setting register *0x463*, bits [7:5], to the desired division value. A value of 0 (default) bypasses the divider entirely.

By default, the divider starts asynchronously. If the application requires synchronization across multiple ADC devices, the SYNC pin provides means for aligning clock dividers to guarantee sampling on the same clock edge. If clock divider is bypassed, this feature is not needed.

Synchronization is enabled by setting register *0x463*, bit [10], to 1. When the bit is 0, SYNC pin is ignored. SYNC is a level sensitive, active high, reset pin that is captured on the falling edge of the input clock. As long as SYNC is high, the divider stays in reset. It starts dividing on the first falling clock edge after SYNC goes low.

Make sure that the falling edge of SYNC meets the specified setup and hold times relative to the input clock, as shown in Table 12. Pay attention to the length matching of the clock and SYNC routing to the multiple ADC chips. For test and debugging purposes, the level of received and captured SYNC signal can be read from register *0x4ff*, bit [10].

Clock Duty-Cycle Requirements. The ADC utilizes both the rising and falling edges of the input clock (or the divided clock, if the divider is enabled) for internal sampling operations. To achieve optimal performance, especially at the maximum sampling rate, the clock duty cycle should be as close to 50% as possible.

When the divider is enabled with an even divisor, a 50% duty cycle is guaranteed by design. If the application uses a clock with a non-ideal duty cycle, a Duty Cycle Stabilizer (DCS) can be enabled to improve performance.

ADC Self-Calibration

The ADC includes an automatic calibration mechanism that is executed at power-up to ensure optimal performance. It calibrates out capacitor mismatch and the effects of operational amplifier finite gain and bandwidth. For best results, calibration should be performed at the actual sampling rate used during operation. To support this, the device continuously monitors the sampling clock frequency and automatically re-triggers calibration if a significant change is detected. This feature can be disabled by setting register *0x4c9*, bit[0], to 1.

Manual calibration can also be initiated by toggling both *0xdc1*, bit[4] and *0xcc1*, bit[4] from 0 to 1. The calibration process is implemented using a state-machine architecture, ensuring a deterministic and predictable calibration time. By default the calibration takes 46 million ADC sampling clock cycles. Calibration completion status can be read from *0xdef*, bit[0] for the first ADC and *0xcef*, bit[0] for the second ADC after the status readback is enabled by writing 0x1c to both *0xdeb* and *0xceb*. Bit value 1 indicates that calibration is complete.

In addition, the ADC supports a Background Calibration (BGC) mode, which is disabled by default. When enabled, paremeters for compensating changes in operational amplifier gain and bandwidth are continuouslty updated. BGC is beneficial in environments with large temperature variations near the hot end of the specified operating temperature range. For its operation, BGC uses a dither signal which is injected into the ADC input signal path. This dither consumes approximately 0.8dB of the ADC's input range, resulting in earlier clipping compared to when BGC is disabled. When BGC is enabled calibration completion staus bit remains 0.

To enable BGC:

- Write 0b01 to register 0xde1, bits [15:14]
- Write 0b01 to register 0xce1, bits [15:14]
- Write 0x0d80 to register 0xdcf
- Write 0x0d80 to register 0xccf
- Write 0b0 to register 0xde3, bit [3]
- Write 0b0 to register 0xce3, bit [3]

Calibration parameters can be altered to optimize ADC performance and the duration of the calibration according to Table Table 17. High Performance settings improve the low frequency SFDR compared to the default settings while the High Speed Settings minimize the calibration time at the cost of small SFDR and SNDR degradation. If the parameters are altered, the calibration has to be reinitiated as described earlier.

Table 17. Calibration Settings.

Register Address	Default Value	High Performance Value	High Speed Value
0xccd	*0x1483*	*0x3483*	*0x348c*
0xcd5	*0x1483*	*0x3483*	*0x348c*
0xcdd	*0x16c3*	*0x36c3*	*0x36cc*
0xce1	*0xbbe8*	*0xbb80*	*0xbb20*
0xdcd	*0x1483*	*0x3483*	*0x348c*
0xdd5	*0x1483*	*0x3483*	*0x348c*
0xddd	*0x16c3*	*0x36c3*	*0x36cc*
0xde1	*0xbbe8*	*0xbb80*	*0xbb20*
Duration (clock cycles)	46M	25M	6.3M

Stand-by and Power-Down Modes

The SD9613 supports two power-saving modes that can be used when the ADC is not actively sampling. In both modes, the SPI interface (if enabled) remains operational.

Power-Down Mode. This mode disables most of the internal circuitry, resulting in the lowest residual supply current. It is ideal for applications requiring minimal power consumption during idle periods. Power-down mode can be enabled via:

- The PDWN pin when operating in the external pin mode, or
- Setting register *0x457*, bit[7], to 1.

Standby Mode. Standby mode offers a faster wake-up time compared to power-down mode, at the cost of slightly higher residual current. It is suitable for applications that require rapid recovery from idle states. To enable standby mode, set register *0x457*, bits [3] and [8], to 1.

Note: It is recommended to disable the ADC auto-calibration when using standby mode to avoid unintended calibration cycles during transitions.

Pin Functions

The SD9613 offers several functions available via dual function pin controls (external pin mode vs. SPI mode). The SD9613 detects the SPI mode during the first SPI transaction after power-up. If the user does not want to program the device via the SPI interface, the dual function is available.

OEB

Output Enable (active-low). If the OEB pin is low, the output data drivers and output clock are enabled. If the OEB pin is high, the LVDS drivers are switched off. The OEB function is not intended for rapid access to a shared data bus.

VCM

Common-Mode Level Bias Output for Analog Input. The VCM pin provides a DC voltage that can be used to bias the ADC input common-mode level, either directly using a passive circuit or indirectly as a common-mode reference voltage for the driving active device. In most use cases, the default common-mode voltage level is optimal. The common-mode voltage level can be changed by register *0xf11*, bits [4:3].

Internal Reference Voltage

The internal vref can be adjusted with *0x45d* bits [4:1]. Usually the default value yields the optimal performance.

SERIAL PORT INTERFACE

The SD9613 uses a 3-wire Serial Port Interface (SPI) that gives the user flexibility to configure the converter for specific functions, depending on the application, through a register space provided inside the ADC. The interface signals are:

- SCLK defines the bit rate at which serial data is driven onto, and sampled from, the bus;
- CSB defines the boundaries of a basic data 'unit', comprised of multiple serial bits;
- SDIO is the serial data IO wire;

The read and write cycles are described in the figure below. The complete instruction cycle is 32-bits long. The falling edge of CSB combines with the rising edge of SCLK marks the start of the instruction cycle. The address space is 13 bits long (A<12:0>) and the data is 16 bits wide (D<15:0>).

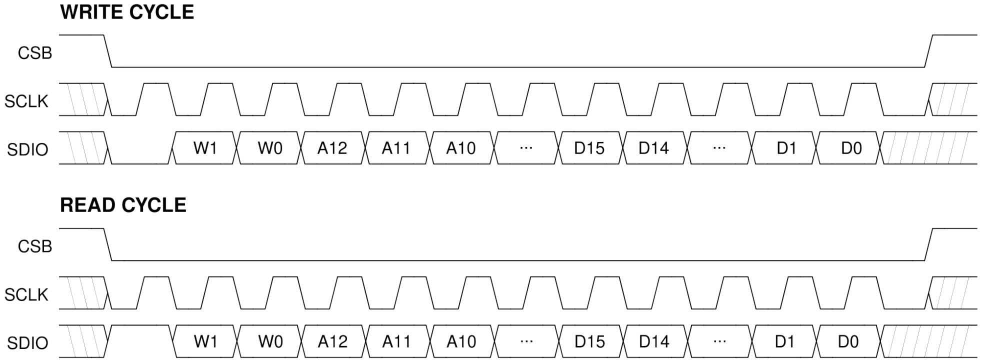


Figure 27: 3-wire SPI timing.

Table 18. SPI Timing.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Setup time between the data and the rising edge of SCLK	t_{DS}	2			ns
Hold time between the data and the rising edge of SCLK	t_{HD}	2			ns
Period of the SCLK	t_{SCLK}	40			ns
Setup time between CSB and SCLK	$t_{S,CSB\text{-}SCLK}$	2			ns
Hold time between CSB and SCLK	$t_{H,CSB\text{-}SCLK}$	2			ns
Minimum period that SCLK should be in a logic high state	$t_{SCLK,high}$	10			ns
Minimum period that SCLK should be in a logic low state	$t_{SCLK,low}$	10			ns
Time from SCLK falling edge to SDIO switching from input to output	$t_{SDIO,EN}$	10			ns
Time from SCLK falling edge to SDIO switching from output to input	$t_{SDIO,DIS}$	10			ns

Two bits, W1 and W0, determine how many bytes of data that can be transferred in the same write cycle (see Table 19). If more than 16 bits (2 Bytes) of data are being transferred the address is increased sequentially.

Table 19. SPI Word Length.

[W1,W0]	Data length
00	Not supported
01	Two bytes of data can be transferred
10	Not supported
11	Four bytes of data can be transferred

The SPI pins should not be active when the full dynamic performance of the ADC is required. Noise from SCLK, CSB and the data transactions can degrade ADC performance.

OUTPUT MODE

Data Scrambler

Interference originating from the digital outputs of the ADC can be difficult to eliminate entirely. Such interference may result from capacitive or inductive coupling mechanisms, or from shared impedance paths in the ground plane. Even minimal coupling coefficients can introduce deterministic spurious tones into the ADC's output frequency spectrum. To mitigate this, digital output scrambling techniques can be employed prior to off-chip transmission. By randomizing the bit patterns, the spectral energy of these spurs is dispersed, effectively reducing their peak amplitudes and minimizing their impact on signal integrity.

The SD9613 can apply an exclusive-OR logic operation between the LSB and all other data output bits, while the LSB, overflow and clock outputs are not affected.

When this function is used, the receiver must apply the same function to unscramble the received data.

The data scrambler is enabled by programming control register *0x4b5*, bit[13].

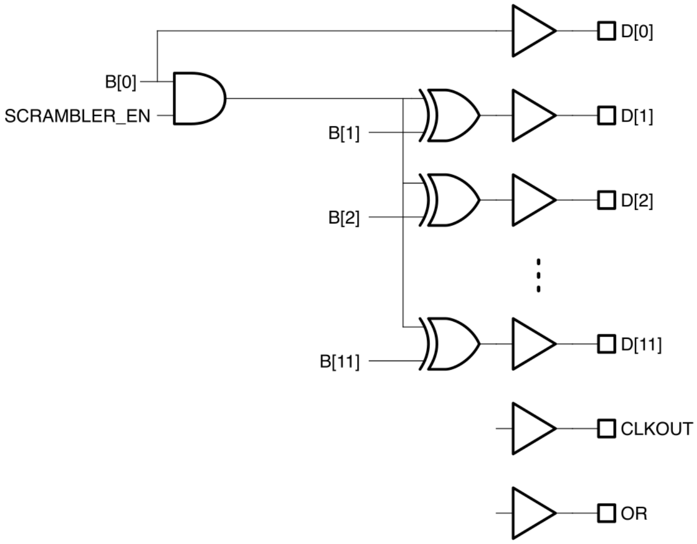


Figure 28: SD9613 Data Scrambler.

Alternate Bit Polarity

The alternate bit polarity is particularly effective to suppress digital feedback and minimize noise coupling on the PCB when the ADC input signal is near mid-scale and of very small amplitude. In this case, the digital output tends to toggle between patterns dominated by either logic high or logic low states. This synchronized switching of multiple bits can induce significant transient currents in the ground plane, leading to increased digital noise. This mode, when activated, inverts all odd-numbered data output bits prior to the output buffer stage while even-numbered bits, along with the overflow and clock output, remain unaffected thus ensuring that approximately half of the output bits transition are high while the other half transition are low. This balanced switching behavior helps cancel out opposing current flows in the ground return path, thereby reducing overall ground noise. At the receiving end, the original data can be reconstructed by inverting the same odd-numbered bits. This mode operates independently of the digital output randomization feature, both functions can be enabled or disabled separately. The Alternate Bit Polarity mode is configured via serial programming of control register *0x4b5*, bit[14].

Output Test Modes

The output test options are described in Table 20 and are selected via SPI programming at register *0x4b5*, bits [5:2].

When an output test mode is enabled, the analog section of the ADC is disconnected from the digital back-end blocks and the test pattern is run through the output formatting block. These tests require an active input clock.

There are two pseudo-random number generators available, PN23 and PN9. The PN23 generator ($X^{23}+X^{18}+1$), selected by register *0x4b5*, bits [5:2], set to 0x5, can be reset by setting register *0x4b5*, bit [12], low; while the PN9 generator ($X^{9}+X^{5}+1$), selected by register *0x4b5* set to 0x6, can be reset by setting register *0x4b5*, bit [11], low.

Table 20. Output Test Modes.

Mode	Function
0	Pass-Through
1	Midscale
2	+FS
3	-FS
4	Checkerboard
5	PN23
6	PN9
7	1/0 word toggle
8	User input
9	1/0 bit toggle
10	1x sync
11	1-bit high
12	Mixed frequency
13	Unused
14	Unused
15	Ramp

Pass-through and test patterns 1, 2, 3, 5 and 6 are subject to output formatting, while the other test modes are not. Test patterns 1, 8 and 15 can be applied to either one channel or both channels using *0x4b5*, bit[7:6]. Patterns 4 and 7 can be toggled between the pattern and its inverse while test pattern 8 can be selected using registers *0x4bb*, *0x4bd*, *0x4bb* and *0x4bb*.

CONTROL REGISTERS

In this section the control registers are described. The template for each register is as follows:

Address: <HEX value>		**RW** or **RO**	**Default: <HEX value>**
bit field	default value	field description.	

where: **RW** indicates a Read/Write register and **RO** indicates a Read-Only register. If the register is read-only, the default value is omitted.

Registers not explicitly described in the following tables should not be written.

When changing control register values, read-modify-write procedure should be used. Some registers contain reserved bit fields for engineering purposes. This avoids inadvertently changing the values of those bits.

0x400 - CHIP_TOP

Address: 0x455		**RW**	**Default: 0x1**
[0]	0x1	Soft reset (active low).	

Address: 0x457		**RW**	**Default: 0x015**
[0]	0x1	Duty Cycle Stabilizer enable.	
[1]	0x0	Duty Cycle Stabilizer on/off in SPI mode.	
[2]	0x1	External output enable (OE/OEB) control 0: Output Enabled 1: Output depends on pin OE/OEB	
[3]	0x0	Output disable 0: Output depends on OE/OEB control and OE/OEB pin 1: Disabled	
[6:4]	0x1	Reserved.	
[7]	0x0	Software power down.	
[8]	0x0	Software sleep mode.	

Address: 0x45d		**RW**	**Default: 0x0095**
[0]	0x1	ADC reference voltage enable.	
[4:1]	0xa	ADC reference voltage value.	
[5]	0x0	Set reference. 0: Internal 1: External from VREF pin	
[11:6]	0x2	Reserved.	
[12]	0x0	Enable Internal vs. External VREF selection using bit 5.	
[13]	0x0	Enable VREF out selection using bit 14.	
[14]	0x0	Enable VREF pin as reference voltage output.	

Address: 0x463		**RW**	**Default: 0x019**
[0]	0x1	Enable clock receiver.	
[2:1]	0x0	Clock RX common-mode voltage bias.	
[4:3]	0x3	Clock RX input stage bias current.	
[7:5]	0x0	Clock RX divider control. 0: Bypass 1: Divide by 2 ... 7: Divide by 8	
[8]	0x0	Enable on-chip 100Ohm termination.	
[9]	0x0	Clock polarity coltrol when DCS is enabled.	
[10]	0x0	Enable SYNC pin synchronization.	

Address: 0x465		**RW**	**Default: 0x0**
[2:0]	0x0	Output data interleaver. 0: pass through, no interleaving 1: pass through, channels swapped, no interleaving 2: N/A 3: N/A 4: parallel ADC_A/ADC_B interleaving 5: parallel ADC_B/ADC_A interleaving 6: even-odd interleaving 7: odd-even interleaving	

Address: 0x467		**RW**	**Default: 0x3850**
[0]	0x0	LVDS enable.	
[1]	0x0	LVDS reduced swing mode.	
[10:2]	0x000	Reserved.	
[13:11]	0x7	LVDS amplitude.	
[15:14]	0x0	Reserved.	

Address: 0x473		**RW**	**Default: 0x0000**
[9:0]	0x0	Reserved.	
[13:10]	0x0	Output clock delay.	
[14]	0x0	Output clock polarity.	

Address: 0x475		**RW**	**Default: 0x1**
[0]	0x1	Enable VCM.	

Address: 0x4b5		RW	Default: 0x18c0
[1:0]	0x0	Output format. 0: Offset binary 1: Signed binary 2: Gray code 3: N/A	
[5:2]	0x0	Output test mode select (see Table 20).	
[6]	0x1	Output test channel CH. A 0: Disable 1: Enable	
[7]	0x1	Output test channel CH. B 0: Disable 1: Enable	
[8]	0x0	Output test toggle mode. Toggle between user test pattern 0 and 1.	
[10:9]	0x0	Reserved.	
[11]	0x1	PN9 generator reset (active low)	
[12]	0x1	PN23 generator reset (active low)	
[13]	0x0	Enable the output data scrambler.	
[14]	0x0	Enable alternate bit polarity switch.	

Address: 0x4b7		RW	Default: 0x0092
[15:0]	0x0092	PN9 initial seed.	

Address: 0x4b9		RW	Default: 0x3aff
[15:0]	0x3aff	PN9 initial seed.	

Address: 0x4bb		RW	Default: 0x0000
[15:0]	0x0000	User test pattern 0 (CH. A).	

Address: 0x4bb		RW	Default: 0x0000
[15:0]	0x0000	User test pattern 1 (CH. A).	

Address: 0x4bf		RW	Default: 0x0000
[15:0]	0x0000	User test pattern 0 (CH. B).	

Address: 0x4c1		RW	Default: 0x0000
[15:0]	0x0000	User test pattern 1 (CH. B).	

Address: 0x4c9		RW	Default: 0x0000
[0]	0x0	Disable auto-recalibration.	
[15:1]	0x0000	Reserved.	

Address: 0x4cf		RW	Default: 0x0035
[0]	0x1	Clock RX second stage bias curret bit [0].	
[1]	0x0	Reserved.	
[2]	0x1	Clock RX second stage bias curret bit [1].	
[14:3]	0x006	Reserved.	
[15]	0x0	Disable production test mode.	

Address: 0x4d3		RW	Default: 0x07
[3:0]	0x7	LVDS common mode voltage.	
[7:4]	0x0	Reserved.	

Address: 0x4fd	RO	Default: N/A
[2:0]	Chip revision.	
[6:3]	Label ID.	
[8:7]	Reserved.	
[10:9]	Resolution ID for device 0: 10-bit 1: 12-bit 2: 14-bit 3: 16-bit	
[13:11]	Speed ID for device.	

Address: 0x4ff	RO	Default: N/A
[0]	Reserved.	
[1]	Analog Supply Ready.	
[2]	Digital Supply Ready.	
[3]	I/O Supply Ready.	
[4]	Reserved.	
[5]	SPI enabled.	
[6]	Power down pin status.	
[9:7]	Reserved.	
[10]	SYNC pin status.	

0xF00 - ADC_DUAL

Address: 0xf03		RW	Default: 0x7f8
[0]	0x0	Enable top level bias.	
[2:1]	0x0	Reserved.	
[3]	0x1	ADC_B enable.	
[10:5]	0x3f	Mask for enable pin.	

Address: 0xf05		RW	Default: 0x30
[5:0]	0x30	Mask for sleep pin.	
[6]	0x0	Sleep ADC_B.	
[7]	0x0	Sleep ADC_A.	

Address: 0xf07		RW	Default: 0x40
[0]	0x0	Digital clock enable.	
[1]	0x0	Analog clock enable.	
[2]	0x0	Reserved.	
[3]	0x0	Clock select.	
[5:4]	0x0	Reserved. 0: ADC_B 1: ADC_A	
[6]	0x1	ADC clock generator reset.	
[7]	0x0	Reserved.	

Address: 0xf09		RW	Default: 0x40
[2:0]	0x0	Channel B source 001: ADC B (default) 011: ADC A 111: (ADC A + ADC B)/2	
[5:3]	0x0	Channel A source 001: ADC A (default) 011: ADC B 111: 0	
[6]	0x1	Reserved.	

Address: 0xf0b		RW	Default: 0x24
[2:0]	0x4	Reserved.	
[5:3]	0x4	ADC master bias.	

Address: 0xf11		RW	Default: 0x0b
[2:0]	0x3	Main bias.	
[4:3]	0x1	VCM voltage control.	

0xDC0 - ADC_A

Address: 0xdc1		RW	Default: 0xbfff
[0]	0x1	Enable.	
[1]	0x1	Clock enable.	
[2]	0x1	Soft reset.	
[3]	0x1	Reserved.	
[4]	0x1	Calibration soft reset.	
[6:5]	0x3	Reserved.	
[10:7]	0xf	Enable mask for en_adc pin.	
[15:11]	0x17	Sleep mask for sleep pin.	

Address: 0xdc3		RW	Default: 0x0000
[3:0]	0x0	Clock phase.	
[11:4]	0x00	Sampling clock fine delay.	
[12]	0x0	Enable fine delay register control.	
[14:13]	0x0	Reserved.	

Address: 0xdc9		RW	Default: 0x6a5
[0]	0x1	Stg1 gain error calibration enable.	
[1]	0x0	Stg1 gain error calibration only.	
[8:2]	0x29	Reserved.	
[9]	0x1	Stg1 enable background mode.	
[11:10]	0x1	Reserved.	

Address: 0xdcd		RW	Default: 0x1483
[2:0]	0x3	Stg1 calibration convergence speed in foreground mode.	
[11:3]	0x090	Reserved.	
[13:12]	0x1	Stg1 calibration randomization sequence in foreground mode.	

Address: 0xdcf		**RW**	**Default: 0xd85**
[2:0]	0x5	Stg1 calibration convergence speed in background mode.	
[11:3]	0x1b0	Reserved.	

Address: 0xdd1		**RW**	**Default: 0x2a5**
[0]	0x1	Stage 2 gain error calibration enable.	
[1]	0x0	Stage 2 gain error calibration only.	
[8:2]	0x29	Reserved.	
[9]	0x1	Stg2 enable background mode.	
[11:10]	0x0	Reserved.	

Address: 0xdd5		**RW**	**Default: 0x1483**
[2:0]	0x3	Stg2 calibration convergence speed in foreground mode.	
[11:3]	0x090	Reserved.	
[13:12]	0x1	Stg2 calibration randomization sequence in foreground mode.	

Address: 0xdd7		**RW**	**Default: 0x001**
[2:0]	0x1	Stg2 calibration convergence speed in background mode.	
[11:3]	0x0	Reserved.	

Address: 0xdd9		**RW**	**Default: 0x0a5**
[0]	0x1	Stg3 gain error calibration enable.	
[1]	0x0	Stg3 gain error calibratio only.	
[7:2]	0x29	Reserved.	
[8]	0x0	Stg3 enable background mode.	
[10:9]	0x0	Reserved.	

Address: 0xddd		**RW**	**Default: 0x16c3**
[2:0]	0x3	Stg3 calibration convergence speed in foreground mode.	
[11:3]	0x0d8	Reserved.	
[13:12]	0x1	Stg3 calibration randomization sequence in foreground mode.	

Address: 0xddf		**RW**	**Default: 0x000**
[2:0]	0x0	Stg3 calibration convergence speed in background mode.	
[11:3]	0x0	Reserved.	

Address: 0xde1		**RW**	**Default: 0xbb28**
[7:0]	0x28	Time allocated for calibration.	
[8]	0x1	Enable calibration.	
[9]	0x1	Enable foreground calibration.	
[10]	0x0	Reserved.	
[11]	0x1	Enable stg1 calibration.	
[12]	0x1	Enable stg2 calibration.	
[13]	0x1	Enable stg3 calibration.	
[14]	0x1	Background calibration parallel mode.	
[15]	0x1	Disable background calibration mode for all stages.	

Address: 0xde3		**RW**	**Default: 0x8**
[2:0]	0x0	Reserved.	
[3]	0x1	Clipping control to reserve some headroom for background calibration signals. Active low.	

Address: 0xde7		**RW**	**Default: 0x04**
[2:0]	0x4	Reserved.	
[4:3]	0x0	Output data timing.	

Address: 0xdeb		**RW**	**Default: 0x00**
[7:0]	0x00	Testbus MUX control.	

Address: 0xdef	**RO**	**Default: N/A**
[15:0].	Testbus read-back register.	

0xCC1 - ADC_B

Address: 0xcc1		**RW**	**Default: 0xbfff**
[0]	0x1	Enable.	
[1]	0x1	Clock enable.	
[2]	0x1	Soft reset.	
[3]	0x1	Reserved.	
[4]	0x1	Calibration soft reset.	
[6:5]	0x3	Reserved.	
[10:7]	0xf	Enable mask for en_adc pin.	
[15:11]	0x17	Sleep mask for sleep pin.	

Address: 0xcc3		**RW**	**Default: 0x0000**
[3:0]	0x0	Clock phase.	
[11:4]	0x00	Sampling clock fine delay.	
[12]	0x0	Enable fine delay register control.	
[14:13]	0x0	Reserved.	

Address: 0xcc9		**RW**	**Default: 0x6a5**
[0]	0x1	Stg1 gain error calibration enable.	
[1]	0x0	Stg1 gain error calibration only.	
[8:2]	0x29	Reserved.	
[9]	0x1	Stg1 enable background mode.	
[11:10]	0x1	Reserved.	

Address: 0xccd		**RW**	**Default: 0x1483**
[2:0]	0x3	Stg1 calibration convergence speed in foreground mode.	
[11:3]	0x090	Reserved.	
[13:12]	0x1	Stg1 calibration randomization sequence in foreground mode.	

Address: 0xccf		**RW**	**Default: 0xd85**
[2:0]	0x5	Stg1 calibration convergence speed in background mode.	
[11:3]	0x1b0	Reserved.	

Address: 0xcd1	**RW**	**Default: 0x2a5**
[0]	0x1	Stage 2 gain error calibration enable.
[1]	0x0	Stage 2 gain error calibration only.
[8:2]	0x29	Reserved.
[9]	0x1	Stg2 enable background mode.
[11:10]	0x0	Reserved.

Address: 0xcd5	**RW**	**Default: 0x1483**
[2:0]	0x3	Stg2 calibration convergence speed in foreground mode.
[11:3]	0x090	Reserved.
[13:12]	0x1	Stg2 calibration randomization sequence in foreground mode.

Address: 0xcd7	**RW**	**Default: 0x001**
[2:0]	0x1	Stg2 calibration convergence speed in background mode.
11:3]	0x0	Reserved.

Address: 0xcd9	**RW**	**Default: 0x0a5**
[0]	0x1	Stg3 gain error calibration enable.
[1]	0x0	Stg3 gain error calibratio only.
[7:2]	0x29	Reserved.
[8]	0x0	Stg3 enable background mode.
[10:9]	0x0	Reserved.

Address: 0xcdd	**RW**	**Default: 0x16c3**
[2:0]	0x3	Stg3 calibration convergence speed in foreground mode.
[11:3]	0x0d8	Reserved.
[13:12]	0x1	Stg3 calibration randomization sequence in foreground mode.

Address: 0xcdf	**RW**	**Default: 0x000**
[2:0]	0x0	Stg3 calibration convergence speed in background mode.
[11:3]	0x0	Reserved.

Address: 0xce1	**RW**	**Default: 0xbb28**
[7:0]	0x28	Time allocated for calibration.
[8]	0x1	Enable calibration.
[9]	0x1	Enable foreground calibration.
[10]	0x0	Reserved.
[11]	0x1	Enable stg1 calibration.
[12]	0x1	Enable stg2 calibration.
[13]	0x1	Enable stg3 calibration.
[14]	0x1	Background calibration parallel mode.
[15]	0x1	Disable background calibration mode for all stages.

Address: 0xce3	**RW**	**Default: 0x8**
[2:0]	0x0	Reserved.
[3]	0x1	Clipping control to reserve some headroom for background calibration signals. Active low.

Address: 0xce7		RW	Default: 0x04
[2:0]	0x4	Reserved.	
[4:3]	0x0	Output data timing.	

Address: 0xceb		RW	Default: 0x00
[7:0]	0x00	Testbus MUX control.	

Address: 0xcef	RO	Default: N/A
[15:0].	Testbus read-back register.	

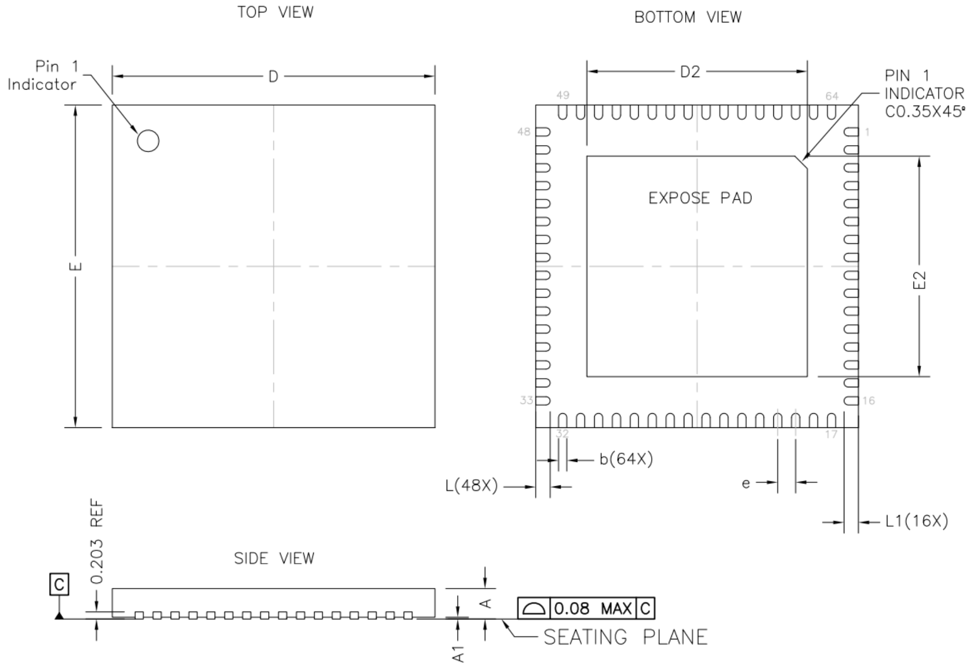
ORDERING INFORMATION

Base Part No.	Orderable Part No. Full Tray	Orderable Part No. Tray with 50Pcs	Orderable Part No. Reel with 750pcs
SD9613-170	SD9613-170-A-QC9-TB	SD9613-170-A-QC9-TA	SD9613-170-A-QC9-RD

EVK	Part No.
LVDS	SDE1117-L

This product is protected by several U.S. Patents (www.silannasemi.com/patents).

PACKAGE DRAWING



DIMENSION TABLE			
SYMBOL	MINIMUM	NOMINAL	MAXIMUM
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.20	0.25	0.30
D	8.90	9.00	9.10
D2	6.10	6.15	6.20
E	8.90	9.00	9.10
E2	6.10	6.15	6.20
e	0.50 BSC		
L	0.35	0.40	0.45
L1	0.33	0.38	0.43

NOTE:

1. Dimensioning and tolerancing conform to ASME Y14.5–2009
2. All dimensions are in millimeters
3. N is the total number of terminals
4. Unilateral coplanarity zone applies to the exposed pas as well as the terminals
5. Lead Finish: 100% Sn

Figure 29: Package Dimensions.

REVISION HISTORY

Version	Date	Comment
1.0	June 19, 2025	Initial Release.
2.0	July 30, 2025	Filled missing specifications. Changed RBIAS resistor to 30kΩ. Improved timing diagrams. Fixed typos.
3.0	November 5, 2025	Updated performance limits. Grouped similar pins together in pinout table. Added IO conversion table. Fixed typos.
4.0	December 9, 2025	Fixed typo in Calibration Settings table.