

SD2184 OVERVIEW

The SD2184 is the dual-channel, 16-bit, analog-to-digital converter (ADC) supporting sampling rates up to 105MSps. The device uses a multistage pipeline architecture to achieve high signal-to-noise ratio (SNR) and linearity, over wide input signal bandwidth. The SD2184 can be set to operate using either CMOS or LVDS output interface. Programming for configuration and control is accomplished using a 4-wire SPI-compatible serial bus. The digital output data can be programmed to be delivered in offset binary, twos complement format, or gray code.

FEATURES

- SNR: 74.7dBFS at $f_{IN} = 70.2\text{MHz}$ and $f_s = 105\text{MSps}$
- SFDR: 89.0dBc at $f_{IN} = 70.2\text{MHz}$ and $f_s = 105\text{MSps}$
- -153.7dBFS/Hz input-noise at $f_{IN} = 70.2\text{MHz}$ and $f_s = 105\text{MSps}$
- $2.0V_{p-p}$ nominal input
- Typical power consumption: 380mW at 105MSps
- Integer 1-to-8 input clock divider (840MHz maximum input rate)
- Sample rates of up to 105MSps
- 1.8V analog supply voltage
- LVDS (ANSI-644 levels) outputs
- Internal ADC voltage reference
- ADC clock duty cycle correction
- Serial port control
- Energy saving power-down modes

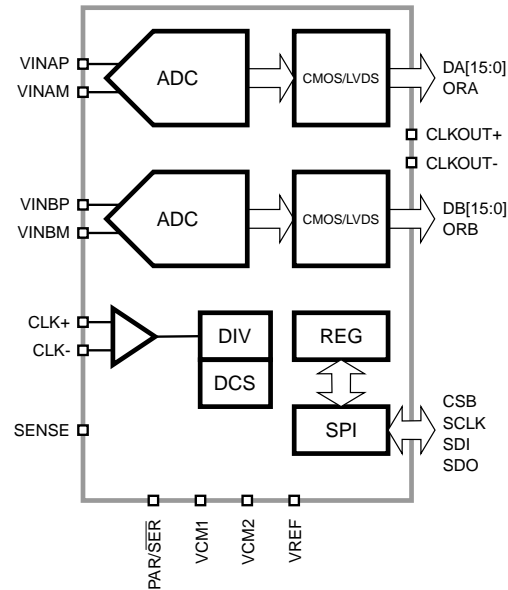


Figure 1: SD2184 Functional Block Diagram.

APPLICATIONS

- Communications
- General-purpose software radios
- I/Q demodulation systems
- Diversity radio systems
- Smart antenna systems
- Multimode digital receivers
- Ultrasound equipment
- Radar/LiDAR applications
- Test and Measurement
- Broadband data applications

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SPECIFICATIONS

DC Specifications

At $T_A = 25^\circ\text{C}$, $V_{DD} = 1.8\text{V}$, $V_{OVDD} = 1.8\text{V}$, $F_{CLK} = 105\text{MHz}$, $A_{IN} = -1\text{dBFS}$, differential AC-coupled external clock source, LVDS mode, unless otherwise noted.

Table 1. DC Specifications.

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
Resolution			16		bits
Accuracy					
Offset Error	Full	-0.50		0.50	%FSR
Gain Error	Full	-3.50		1.50	%FSR
DNL	Full			± 2.5	LSB
INL	Full			± 8.0	LSB
Matching					
Offset Error	25°C	-0.80		0.80	%FSR
Gain Error	25°C	-0.40		0.40	%FSR
Temperature Drift					
Offset Error	Full		± 0.5		ppm/°C
Gain Error	Full		80.0		ppm/°C
Internal Voltage Reference					
Output Voltage	Full	1.02		1.07	V
External Voltage Reference					
Range	Full	0.90		1.07	V
Input Referred Noise					
$V_{REF} = 1.0\text{V}$	25°C		3.45		LSB(rms)
Analog Input					
Input Span, $V_{REF}=1.0\text{V}$	Full		2.0		V
Input Capacitance	Full		6.0		pF
Input Resistance	Full		2.0		k Ω
Input Common-Mode Voltage	Full		0.70		V
Input Common-Mode Range	Full	0.62		0.93	V
VCM Voltage	Full		0.65		V
VCM Current Capability	Full		100		μA
Reference Input Resistance	Full		50		k Ω
Power Supply					
V_{DD}	Full	1.7	1.8	1.9	V
V_{OVDD} (CMOS)	Full	1.7	1.8	1.9	V
V_{OVDD} (LVDS)	Full	1.7	1.8	1.9	V
I_{VDD} @1.8V	Full		178	240	mA
I_{OVDD} @1.8V (CMOS)	Full		25	31	mA
I_{OVDD} @1.8V (LVDS)	Full		50	67	mA
Power Consumption					
Sine Wave Input (CMOS)	Full		380		mW
Sine Wave Input (LVDS)	Full		420		mW
Stand-by ¹ (CMOS)	Full		60		mW
Stand-by ¹ (LVDS)	Full		60		mW
Power Down	Full		10.0		mW

¹ Stand-by power is measured with a sinewave input and active clock.

AC Specifications

At $T_A = 25^\circ\text{C}$, $V_{DD} = 1.8\text{V}$, $V_{OVDD} = 1.8\text{V}$, $F_{CLK} = 105\text{MHz}$, $A_{IN} = -1\text{dBFS}$, differential AC-coupled external clock source, High-Performance Calibration Mode enabled, LVDS mode, unless otherwise noted.

Table 2. AC Performance Specifications.

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
Signal-to-Noise Ratio (SNR)					
$f_{IN} = 6.55\text{MHz}$	25°C		76.0		dBFS
$f_{IN} = 70.2\text{MHz}$	25°C		74.7		dBFS
	Full	74.0			dBFS
$f_{IN} = 140\text{MHz}$	25°C		72.6		dBFS
$f_{IN} = 220\text{MHz}$	25°C		69.8		dBFS
Signal-to-Noise and Distortion Ratio (SNDR)					
$f_{IN} = 6.55\text{MHz}$	25°C		75.6		dBFS
$f_{IN} = 70.2\text{MHz}$	25°C		74.5		dBFS
	Full	73.2			dBFS
$f_{IN} = 140\text{MHz}$	25°C		72.3		dBFS
$f_{IN} = 220\text{MHz}$	25°C		69.3		dBFS
Effective Number of Bits (ENOB)					
$f_{IN} = 6.55\text{MHz}$	25°C		12.3		bits
$f_{IN} = 70.2\text{MHz}$	25°C		12.1		bits
$f_{IN} = 140\text{MHz}$	25°C		11.7		bits
$f_{IN} = 220\text{MHz}$	25°C		11.2		bits
Worst 2 nd or 3 rd Harmonic Power					
$f_{IN} = 6.55\text{MHz}$	25°C		-93.0		dBc
$f_{IN} = 70.2\text{MHz}$	25°C		-86.0	-85.0	dBc
$f_{IN} = 140\text{MHz}$	25°C		-87.0		dBc
$f_{IN} = 220\text{MHz}$	25°C		-82.0		dBc
Worst Non-Harmonic Power					
$f_{IN} = 6.55\text{MHz}$	25°C		-93.0		dBc
$f_{IN} = 70.2\text{MHz}$	25°C		-87.0	-88.0	dBc
$f_{IN} = 140\text{MHz}$	25°C		-88.0		dBc
$f_{IN} = 220\text{MHz}$	25°C		-82.0		dBc
Spurious-Free Dynamic Range ¹ (SFDR)					
$f_{IN} = 6.55\text{MHz}$	25°C		93.0		dBc
$f_{IN} = 70.2\text{MHz}$	25°C		89.0		dBc
	Full	82.0			dBc
$f_{IN} = 140\text{MHz}$	25°C		87.0		dBc
$f_{IN} = 220\text{MHz}$	25°C		82.0		dBc
Two-Tone SFDR					
$f_{IN1} = 29.1\text{MHz}$, $f_{IN2} = 30.6\text{MHz}$	25°C		90.7		dBc
Crosstalk ²	25°C		-105.0		dBc
Analog Input Bandwidth	Full		650.0		MHz

¹ SFDR excludes the DC and $f_s/2$ bins.

² Crosstalk is measured at 100MHz with -1.0dBFS on one channel and no input on the alternate channel.

Digital Specification

$V_{DD} = 1.8V$, $V_{OVDD} = 1.8V$, $F_{CLK} = 105MHz$, $A_{IN} = -1dBFS$, differential AC-coupled external clock source, DCS disabled, unless otherwise noted.

Table 3. Differential Clock Input.

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
Logic Compliance	Full	CMOS/LVDS/LVPECL			
Internal Common-Mode Bias	Full		0.9		V
Differential Input Voltage	Full	0.3		1.2	V_{p-p}
Input Voltage Range	Full	$V_{GND}-0.3$		$V_{VDD}+0.2$	V
Input Common-Mode Range	Full	0.75		1.05	V
High Level Input Current	Full	-10		10	μA
Low Level Input Current	Full	-10		10	μA
Input Capacitance	Full		1.7		pF
Input Resistance	Full		6.0		k Ω

Table 4. CSB, SDI, SCLK in Serial or Parallel Programming Mode SDO in Parallel Programming Mode.

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
High Level Input Voltage	Full	1.22			V
Low Level Input Voltage	Full			0.6	V
High Level Input Current	Full	-1		1	μA
Low Level Input Current	Full	-1		1	μA
Input Capacitance	Full		1.5		pF
Input Resistance	Full		100		k Ω

Table 5. SDO (Serial Programming Mode).

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
High Level Output Voltage @50 μA	Full	1.77			V
High Level Output Voltage @0.5mA	Full	1.75			V
Low Level Output Voltage @50 μA	Full			0.05	V
Low Level Output Voltage @1.6mA	Full			0.10	V

Table 6. CMOS Outputs.

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
High Level Output Voltage @50 μA	Full	1.77			V
High Level Output Voltage @0.5mA	Full	1.75			V
Low Level Output Voltage @50 μA	Full			0.05	V
Low Level Output Voltage @1.6mA	Full			0.10	V

Table 7. LVDS Outputs.

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
Differential Output Voltage (V_{OD}), ANSI Mode	Full	250	300	450	mV
Output Offset Voltage (V_{OS}), ANSI Mode	Full	1.10	1.22	1.30	V
Differential Output Voltage (V_{OD}), Reduced Swing	Full	150	220	285	mV
Output Offset Voltage (V_{OS}), Reduced Swing	Full	1.10	1.22	1.30	V

Switching Specifications

$V_{DD} = 1.8V$, $V_{OVD} = 1.8V$, $F_{CLK} = 105MHz$, $A_{IN} = -1dBFS$, differential AC-coupled sine wave external clock source, DCS enabled, unless otherwise noted.

Table 8. Clock Input Timing.

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
Input Clock Rate	Full			840	MHz
Conversion Rate (after clock divider)	Full	10.0		105.0	MHz
<i>CLK Pulse Width High (t_{CH})</i>					
Divide-by-1 Mode, DCS Enabled	Full	1.5			ns
Divide-by-1 Mode, DCS Disabled	Full	4.2	4.8	5.2	ns
Divide-by-2 Mode Through Divide-by-8 Mode	Full	0.6			ns
Aperture Delay (t_A)	Full		0.5		ns
Aperture Uncertainty (Jitter, t_J)	Full		140.0		fs

Table 9. Data Output.

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
<i>CMOS Mode</i>					
Data Propagation Delay (t_{PD})	Full		6.0		ns
DCO Propagation Delay (t_{DCO})	Full		7.0		ns
DCO to Data Skew (t_{SKEW})	Full	-2.1	-1.1	-0.1	ns
Pipeline Delay (Latency, L)	Full		35.0		Cycles
<i>LVDS Mode</i>					
Data Propagation Delay (t_{PD})	Full		8.0		ns
DCO Propagation Delay (t_{DCO})	Full		7.7		ns
DCO to Data Skew (t_{SKEW})	Full	-0.5	0.1	0.7	ns
Pipeline Delay (Latency, L) Channel A/Channel B	Full		32/32.5		Cycles
Wake-Up Time (from sleep)	Full		5.0		μs
Wake-Up Time (from power down)	Full		400.0		μs
Out-of-Range Recovery Time	Full		3		Cycles

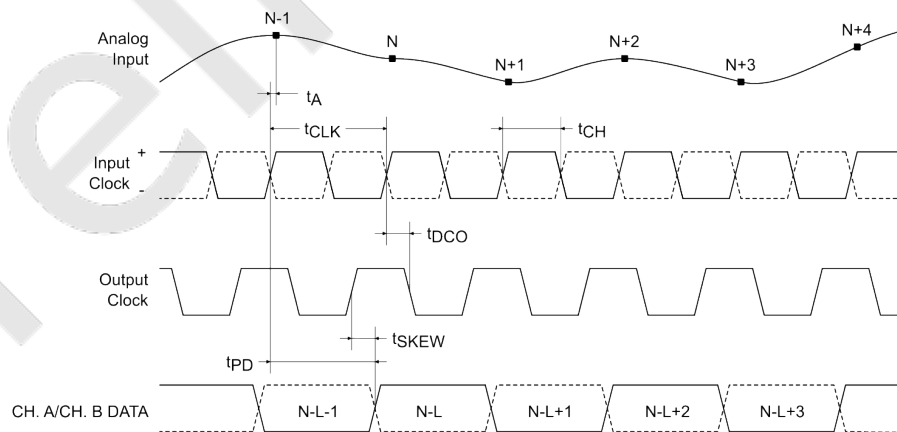


Figure 2: Parallel CMOS Output Mode Timing.

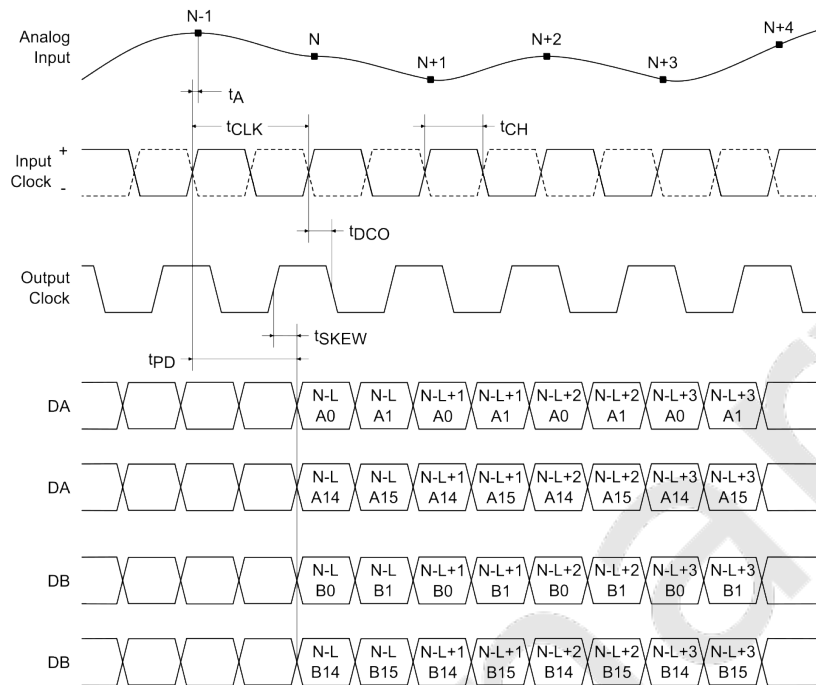


Figure 3: Channel Multiplexed CMOS Output Mode Timing.

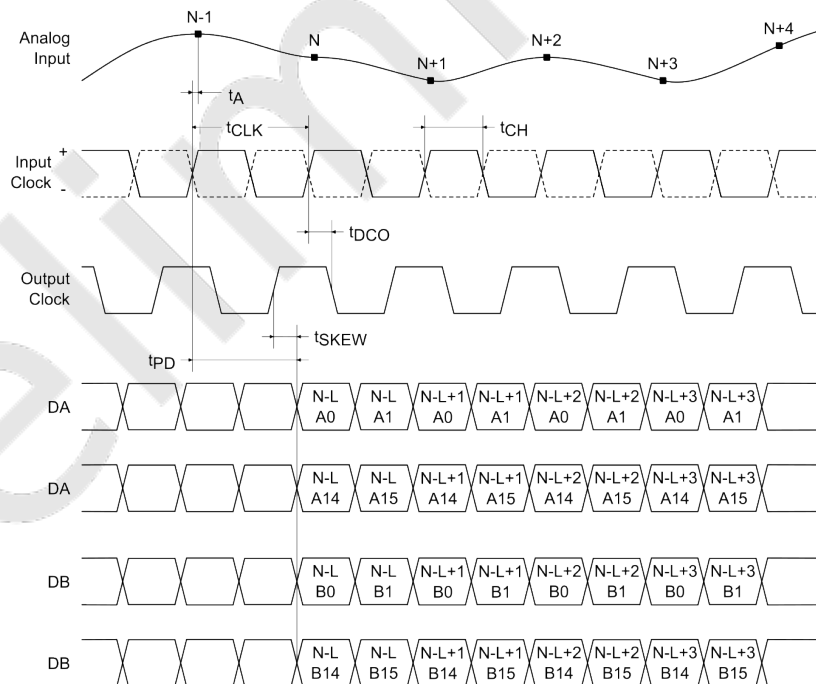


Figure 4: Channel Multiplexed LVDS Output Mode Timing.

Output Modes

The SD2184 supports both CMOS and LVDS interfaces. Two LVDS samples are sent out every clock cycle using both the

rising and the falling edge of the output clock. In interleaved parallel mode, the two ADCs share the full set of output pins. The first half-cycle contains ADC A data and the second ADC B data. In multiplexed mode, each ADC has its dedicated set of output pins and the data is sent out even numbered bits on the first half-cycle and the odd bits on the second.

Output Timing Control

Data delay control, bits [8:5], in register $0x473$, can be used to move the CMOS data relative to output clock. Bit [9] inverts the internal clock sending the data out. Bits [13:10], in register $0x473$, control the output clock delay relative to output data, while bit [14] inverts the clock. The delay step size is about 250ps.

Data delay control is not available in interleaved or multiplexed output mode.

Driving long traces or large load capacitance with CMOS output produces voltage ripple in the digital IO supply and ground, which may couple on chip to the sensitive analog circuits in the ADC and degrade the performance. This effect can be reduced by using an external buffer IC. The use of LVDS output interface largely eliminates issues with IO supply noise.

ABSOLUTE MAXIMUM RATINGS

Table 10. Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$, unless otherwise specified).

Parameter	Symbol	Conditions	Min	Max	Units
VDD	V_{VDD}	Relative to GND	-0.3	2.0	V
OVDD	V_{OVDD}	Relative to GND	-0.3	2.0	V
VINAP/VINBP, VINAM/VINBM		Relative to GND	-0.3	2.0	V
CLK+, CLK-		Relative to GND	-0.3	2.0	V
VCM		Relative to GND	-0.3	2.0	V
VREF		Relative to GND	-0.3	2.0	V
PAR/SER		Relative to GND	-0.3	2.0	V
CSB		Relative to GND	-0.3	2.0	V
SCLK		Relative to GND	-0.3	2.0	V
SDI		Relative to GND	-0.3	2.0	V
SDO		Relative to GND	-0.3	2.0	V
DA0, ..., DA15 DB0, ..., DB15		Relative to GND	-0.3	2.0	V
CLKOUT+, CLKOUT-		Relative to GND	-0.3	2.0	V
Operating Temperature Range (Ambient)			-40	85	°C
Maximum Junction Temperature Under Bias				125	
Storage Temperature Range (Ambient)			-65	150	

Notes:

- Stresses beyond those listed under Table 10 may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

ESD CAUTION.



Electrostatic Discharge Sensitive Device.

Proper ESD precautions should be observed to prevent performance degradation or loss of functionality.

PACKAGE

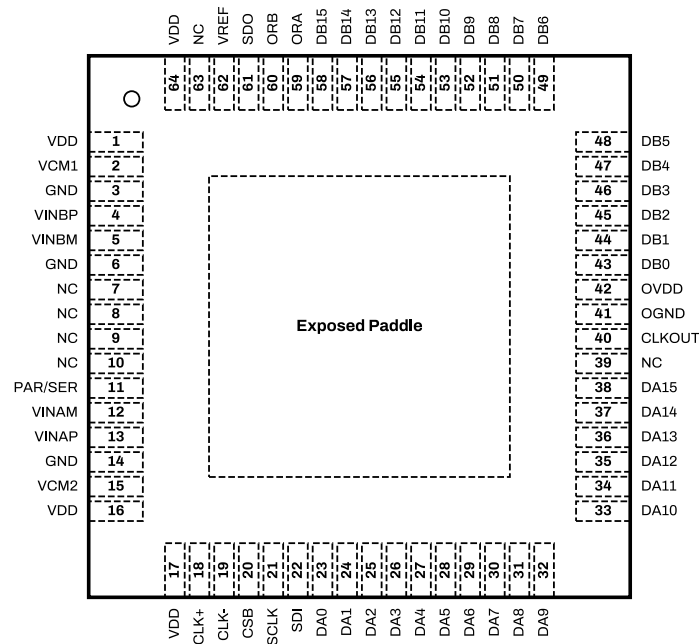


Figure 5: SD2184 Package Top View for Parallel CMOS Configuration.

1. The exposed thermal pad on the bottom of the package provides the analog ground for the part and must be connected for proper operation.

Table 11. Pin Descriptions for Parallel CMOS Configuration.

Number	Name	Type	Comment
0	GND	Ground	Exposed Paddle, Analog Ground.
1, 16, 17, 64	VDD	Power	Analog Supply Voltage.
2	VCM1	Output	Common Mode Bias Output, Nominally Equal to VDD/2. VCM1 should be used to bias the common mode of the analog inputs to channel 1. Bypass to ground with a 0.1uF ceramic capacitor.
3, 6, 14	GND	Ground	ADC Ground.
4	VINBP	Input	Differential Analog Input Pin (Plus) for Channel B.
5	VINBM	Input	Differential Analog Input Pin (Minus) for Channel B.
7, 8, 9, 10, 39, 63	NC		Do not connect.
11	PAR/SER	Input	Programming Mode Selection Pin. Connect to ground to enable the serial programming mode. CS, SCK, SDI, SDO become a serial interface that control the ADC operating modes. Connect to VDD to enable the parallel programming mode where CS, SCK, SDI, SDO become parallel logic inputs that control a reduced set of the A/D operating modes. PAR/SER should be connected directly to ground or VDD and not be driven by a logic signal.
12	VINAM	Input	Differential Analog Input Pin (Minus) for Channel A.
13	VINAP	Input	Differential Analog Input Pin (Plus) for Channel A.

Number	Name	Type	Comment
15	VCM2	Output	Common Mode Bias Output, Nominally Equal to VDD/2. VCM2 should be used to bias the common mode of the analog inputs to channel 2. Bypass to ground with a 0.1uF ceramic capacitor.
18	CLK+	Input	ADC Clock Input (Plus).
19	CLK-	Input	ADC Clock Input (Minus).
20	CSB	Input	SPI Chip Select (Active Low).
21	SCLK	Input	This pin functions as a serial interface clock input when RESET is low. It controls the low-speed mode when RESET is tied high. This pin has an internal pulldown resistor.
22	SDI	Input	In Serial Programming Mode, (PAR/SER = 0V), SDI Is the Serial Interface Data Input. Data on SDI is clocked into the mode control registers on the rising edge of SCK. In the parallel programming mode (PAR/ SER = VDD), SDI can be used together with SDO to power down the part.
23	DA0	Output	Channel A CMOS Output Data 0 (LSB).
24	DA1	Output	Channel A CMOS Output Data 1.
25	DA2	Output	Channel A CMOS Output Data 2.
26	DA3	Output	Channel A CMOS Output Data 3.
27	DA4	Output	Channel A CMOS Output Data 4.
28	DA5	Output	Channel A CMOS Output Data 5.
29	DA6	Output	Channel A CMOS Output Data 6.
30	DA7	Output	Channel A CMOS Output Data 7.
31	DA8	Output	Channel A CMOS Output Data 8.
32	DA9	Output	Channel A CMOS Output Data 9.
33	DA10	Output	Channel A CMOS Output Data 10.
34	DA11	Output	Channel A CMOS Output Data 11.
35	DA12	Output	Channel A CMOS Output Data 12.
36	DA13	Output	Channel A CMOS Output Data 13.
37	DA14	Output	Channel A CMOS Output Data 14.
38	DA15	Output	Channel A CMOS Output Data 15.
40	CLKOUT	Output	Data Output Clock.
41	OGND	Ground	Output Driver Ground. Must be shorted to the ground plane by a very low inductance path. Use multiple vias close to the pin.
42	OVD	Power	Digital I/O Supply. Bypass to ground with a 0.1uF ceramic capacitor.
43	DB0	Output	Channel B CMOS Output Data 0 (LSB).
44	DB1	Output	Channel B CMOS Output Data 1.
45	DB2	Output	Channel B CMOS Output Data 2.
46	DB3	Output	Channel B CMOS Output Data 3.
47	DB4	Output	Channel B CMOS Output Data 4.
48	DB5	Output	Channel B CMOS Output Data 5.
49	DB6	Output	Channel B CMOS Output Data 6.
50	DB7	Output	Channel B CMOS Output Data 7.
51	DB8	Output	Channel B CMOS Output Data 8.
52	DB9	Output	Channel B CMOS Output Data 9.
53	DB10	Output	Channel B CMOS Output Data 10.
54	DB11	Output	Channel B CMOS Output Data 11.
55	DB12	Output	Channel B CMOS Output Data 12.
56	DB13	Output	Channel B CMOS Output Data 13.
57	DB14	Output	Channel B CMOS Output Data 14.

Number	Name	Type	Comment
58	DB15	Output	Channel B CMOS Output Data 15.
59	ORA	Output	Channel A Overrange Output.
60	ORB	Output	Channel B Overrange Output.
61	SDO	Output	In Serial Programming Mode, (PAR/SER = 0V), SDO is the Optional Serial Interface Data Output. In the parallel programming mode (PAR/SER = VDD), SDO can be used together with SDI to power down the part.
62	VREF	InOut	Voltage Reference Input/Output.

Preliminary

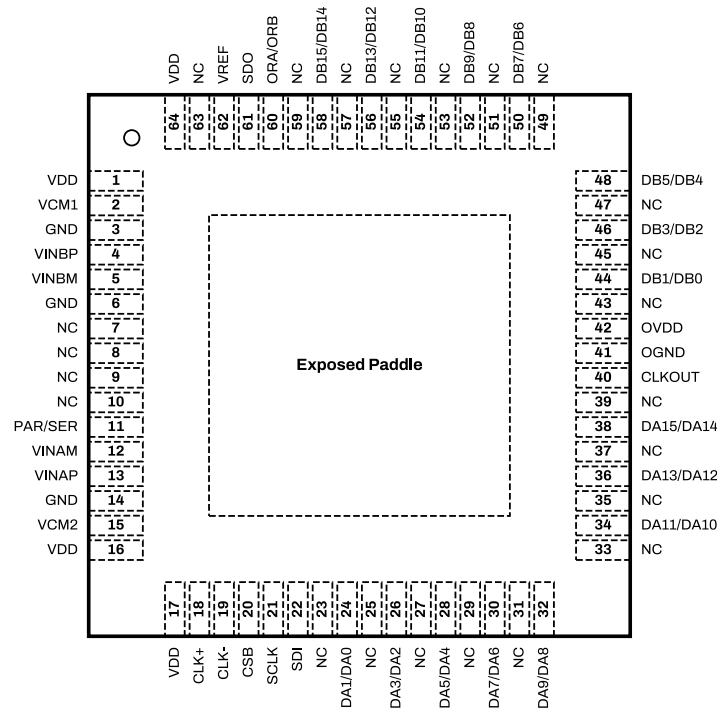


Figure 6: SD2184 Package Top View for Channel Multiplexed CMOS Configuration.

1. The exposed thermal pad on the bottom of the package provides the analog ground for the part and must be connected for proper operation.

Table 12. Pin Descriptions for Channel Multiplexed CMOS Configuration.

Number	Name	Type	Comment
0	GND	Ground	Exposed Paddle, Analog Ground.
1, 16, 17, 64	VDD	Power	Analog Supply Voltage.
2	VCM1	Output	Common Mode Bias Output, Nominally Equal to VDD/2. VCM1 should be used to bias the common mode of the analog inputs to channel 1. Bypass to ground with a 0.1uF ceramic capacitor.
3, 6, 14	GND	Ground	ADC Ground.
4	VINBP	Input	Differential Analog Input Pin (Plus) for Channel B.
5	VINBM	Input	Differential Analog Input Pin (Minus) for Channel B.
7, 8, 9, 10, 23, 25, 27, 29, 31, 33, 35, 37, 39, 43, 45, 47, 49, 51, 53, 55, 57, 59, 63	NC		Do not connect.

Number	Name	Type	Comment
11	PAR/SER	Input	Programming Mode Selection Pin. Connect to ground to enable the serial programming mode. CS, SCK, SDI, SDO become a serial interface that control the ADC operating modes. Connect to VDD to enable the parallel programming mode where CS, SCK, SDI, SDO become parallel logic inputs that control a reduced set of the A/D operating modes. PAR/SER should be connected directly to ground or VDD and not be driven by a logic signal.
12	VINAM	Input	Differential Analog Input Pin (Minus) for Channel A.
13	VINAP	Input	Differential Analog Input Pin (Plus) for Channel A.
15	VCM2	Output	Common Mode Bias Output, Nominally Equal to VDD/2. VCM2 should be used to bias the common mode of the analog inputs to channel 2. Bypass to ground with a 0.1uF ceramic capacitor.
18	CLK+	Input	ADC Clock Input (Plus).
19	CLK-	Input	ADC Clock Input (Minus).
20	CSB	Input	SPI Chip Select (Active Low).
21	SCLK	Input	This pin functions as a serial interface clock input when RESET is low. It controls the low-speed mode when RESET is tied high. This pin has an internal pulldown resistor.
22	SDI	Input	In Serial Programming Mode, (PAR/SER = 0V), SDI is the Serial Interface Data Input. Data on SDI is clocked into the mode control registers on the rising edge of SCK. In the parallel programming mode (PAR/ SER = VDD), SDI can be used together with SDO to power down the part.
24	DA1/DA0	Output	nan
26	DA3/DA2	Output	Channel A CMOS Output Data 2 and 3.
28	DA5/DA4	Output	Channel A CMOS Output Data 4 and 5.
30	DA7/DA6	Output	Channel A CMOS Output Data 6 and 7.
32	DA9/DA8	Output	Channel A CMOS Output Data 8 and 9.
34	DA11/DA10	Output	Channel A CMOS Output Data 10 and 11.
36	DA13/DA12	Output	Channel A CMOS Output Data 12 and 13.
38	DA15/DA14	Output	Channel A CMOS Output Data 14 and 15.
40	CLKOUT	Output	Data Output Clock.
41	OGND	Ground	Output Driver Ground. Must be shorted to the ground plane by a very low inductance path. Use multiple vias close to the pin.
42	OVDD	Power	Digital I/O Supply. Bypass to ground with a 0.1uF ceramic capacitor.
44	DB1/DB0	Output	Channel B CMOS Output Data 0 and 1.
46	DB3/DB2	Output	Channel B CMOS Output Data 2 and 3.
48	DB5/DB4	Output	Channel B CMOS Output Data 4 and 5.
50	DB7/DB6	Output	Channel B CMOS Output Data 6 and 7.
52	DB9/DB8	Output	Channel B CMOS Output Data 8 and 9.
54	DB11/DB10	Output	Channel B CMOS Output Data 10 and 11.
56	DB13/DB12	Output	Channel B CMOS Output Data 12 and 13.
58	DB15/DB14	Output	Channel B CMOS Output Data 14 and 15.
60	ORA/ORB	Output	Channel A/Channel B CMOS Overrange.
61	SDO	Output	In Serial Programming Mode, (PAR/SER = 0V), SDO is the Optional Serial Interface Data Output. In the parallel programming mode (PAR/SER = VDD), SDO can be used together with SDI to power down the part.
62	VREF	InOut	Voltage Reference Input/Output.

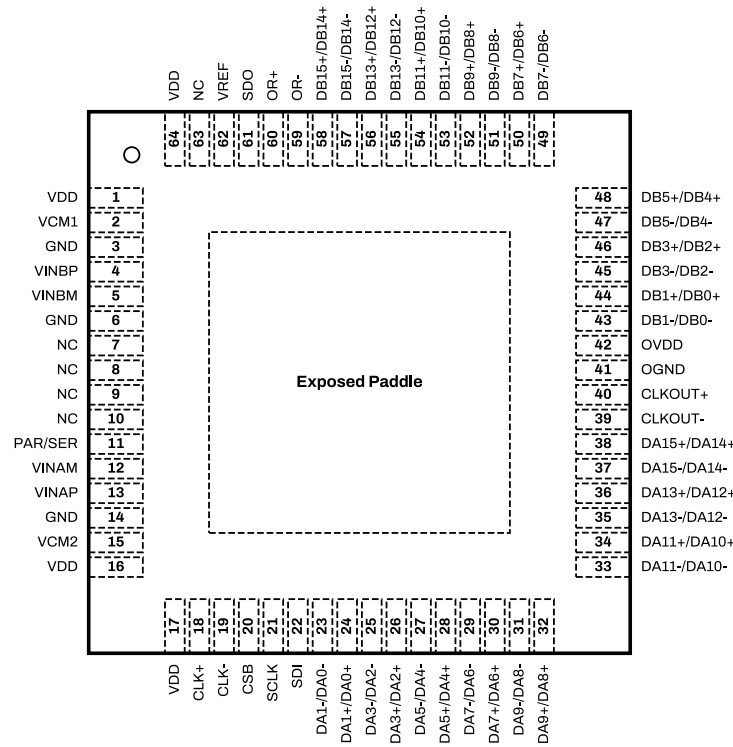


Figure 7: SD2184 Package Top View for Channel Multiplexed LVDS Configuration.

1. The exposed thermal pad on the bottom of the package provides the analog ground for the part and must be connected for proper operation.

Table 13. Pin Descriptions for Channel Multiplexed LVDS Configuration.

Number	Name	Type	Comment
0	GND	Ground	Exposed Paddle, Analog Ground.
1, 16, 17, 64	VDD	Power	Analog Supply Voltage.
2	VCM1	Output	Common Mode Bias Output, Nominally Equal to VDD/2. VCM1 should be used to bias the common mode of the analog inputs to channel 1. Bypass to ground with a 0.1uF ceramic capacitor.
3, 6, 14	GND	Ground	ADC Ground.
4	VINBP	Input	Differential Analog Input Pin (Plus) for Channel B.
5	VINBM	Input	Differential Analog Input Pin (Minus) for Channel B.
7, 8, 9, 10, 63	NC		Do not connect.
11	PAR/SER	Input	Programming Mode Selection Pin. Connect to ground to enable the serial programming mode. CS, SCK, SDI, SDO become a serial interface that control the ADC operating modes. Connect to VDD to enable the parallel programming mode where CS, SCK, SDI, SDO become parallel logic inputs that control a reduced set of the A/D operating modes. PAR/SER should be connected directly to ground or VDD and not be driven by a logic signal.
12	VINAM	Input	Differential Analog Input Pin (Minus) for Channel A.
13	VINAP	Input	Differential Analog Input Pin (Plus) for Channel A.
15	VCM2	Output	Common Mode Bias Output, Nominally Equal to VDD/2. VCM2 should be used to bias the common mode of the analog inputs to channel 2. Bypass to ground with a 0.1uF ceramic capacitor.

Number	Name	Type	Comment
18	CLK+	Input	ADC Clock Input (Plus).
19	CLK-	Input	ADC Clock Input (Minus).
20	CSB	Input	SPI Chip Select (Active Low).
21	SCLK	Input	This pin functions as a serial interface clock input when RESET is low. It controls the low-speed mode when RESET is tied high. This pin has an internal pulldown resistor.
22	SDI	Input	In Serial Programming Mode, (PAR/SER = 0V), SDI is the Serial Interface Data Input. Data on SDI is clocked into the mode control registers on the rising edge of SCK. In the parallel programming mode (PAR/ SER = VDD), SDI can be used together with SDO to power down the part.
23	DA1-/DA0-	Output	Channel A LVDS Output Data 0 and 1 (Minus).
24	DA1+/DA0+	Output	Channel A LVDS Output Data 0 and 1 (Plus).
25	DA3-/DA2-	Output	Channel A LVDS Output Data 2 and 3 (Minus).
26	DA3+/DA2+	Output	Channel A LVDS Output Data 2 and 3 (Plus).
27	DA5-/DA4-	Output	Channel A LVDS Output Data 4 and 5 (Minus).
28	DA5+/DA4+	Output	Channel A LVDS Output Data 4 and 5 (Plus).
29	DA7-/DA6-	Output	Channel A LVDS Output Data 6 and 7 (Minus).
30	DA7+/DA6+	Output	Channel A LVDS Output Data 6 and 7 (Plus).
31	DA9-/DA8-	Output	Channel A LVDS Output Data 8 and 9 (Minus).
32	DA9+/DA8+	Output	Channel A LVDS Output Data 8 and 9 (Plus).
33	DA11-/DA10-	Output	Channel A LVDS Output Data 10 and 11 (Minus).
34	DA11+/DA10+	Output	Channel A LVDS Output Data 10 and 11 (Plus).
35	DA13-/DA12-	Output	Channel A LVDS Output Data 12 and 13 (Minus).
36	DA13+/DA12+	Output	Channel A LVDS Output Data 12 and 13 (Plus).
37	DA15-/DA14-	Output	Channel A LVDS Output Data 14 and 15 (Minus).
38	DA15+/DA14+	Output	Channel A LVDS Output Data 14 and 15 (Plus).
39	CLKOUT-	Output	Inverted Version of CLKOUT+.
40	CLKOUT+	Output	Data Output Clock.
41	OGND	Ground	Output Driver Ground. Must be shorted to the ground plane by a very low inductance path. Use multiple vias close to the pin.
42	OVDD	Power	Digital I/O Supply. Bypass to ground with a 0.1µF ceramic capacitor.
43	DB1-/DB0-	Output	Channel B LVDS Output Data 0 and 1 (Minus).
44	DB1+/DB0+	Output	Channel B LVDS Output Data 0 and 1 (Plus).
45	DB3-/DB2-	Output	Channel B LVDS Output Data 2 and 3 (Minus).
46	DB3+/DB2+	Output	Channel B LVDS Output Data 2 and 3 (Plus).
47	DB5-/DB4-	Output	Channel B LVDS Output Data 4 and 5 (Minus).
48	DB5+/DB4+	Output	Channel B LVDS Output Data 4 and 5 (Plus).
49	DB7-/DB6-	Output	Channel B LVDS Output Data 6 and 7 (Minus).
50	DB7+/DB6+	Output	Channel B LVDS Output Data 6 and 7 (Plus).
51	DB9-/DB8-	Output	Channel B LVDS Output Data 8 and 9 (Minus).
52	DB9+/DB8+	Output	Channel B LVDS Output Data 8 and 9 (Plus).
53	DB11-/DB10-	Output	Channel B LVDS Output Data 10 and 11 (Minus).
54	DB11+/DB10+	Output	Channel B LVDS Output Data 10 and 11 (Plus).
55	DB13-/DB12-	Output	Channel B LVDS Output Data 12 and 13 (Minus).
56	DB13+/DB12+	Output	Channel B LVDS Output Data 12 and 13 (Plus).
57	DB15-/DB14-	Output	Channel B LVDS Output Data 14 and 15 (Minus).
58	DB15+/DB14+	Output	Channel B LVDS Output Data 14 and 15 (Plus).
59	OR-	Output	Channel A/Channel B LVDS Overage (Minus).

Number	Name	Type	Comment
60	OR+	Output	Channel A/Channel B LVDS Overrange (Plus).
61	SDO	Output	In Serial Programming Mode, (PAR/SER = 0V), SDO is the Optional Serial Interface Data Output. In the parallel programming mode (PAR/SER = VDD), SDO can be used together with SDI to power down the part.
62	VREF	InOut	Voltage Reference Input/Output.

Preliminary

TYPICAL PERFORMANCE CHARACTERISTICS

At $T_A = 25^\circ\text{C}$, $V_{DD} = 1.8\text{V}$, $V_{OVD} = 1.8\text{V}$, $F_{CLK} = 105\text{MHz}$, $A_{IN} = -1\text{dBFS}$, differential AC-coupled clock source, High-Performance Calibration Mode enabled, LVDS mode, unless otherwise noted.

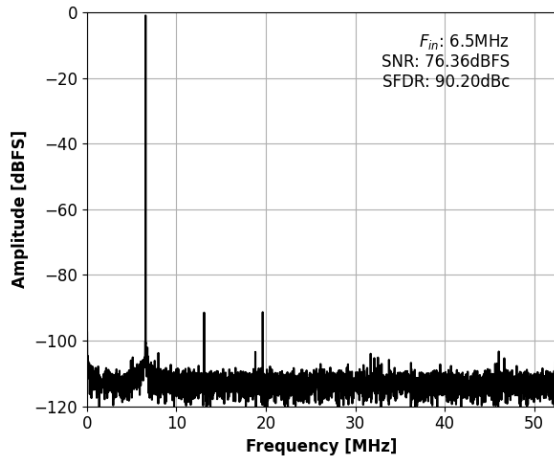


Figure 8: Single-Tone FFT with $f_{IN}=6.55\text{MHz}$.

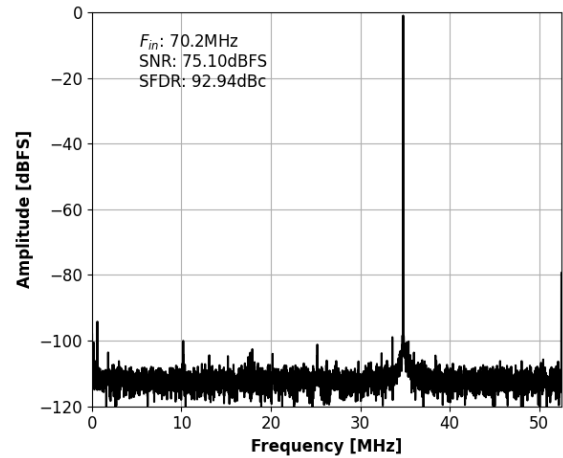


Figure 9: Single-Tone FFT with $f_{IN}=70.2\text{MHz}$.

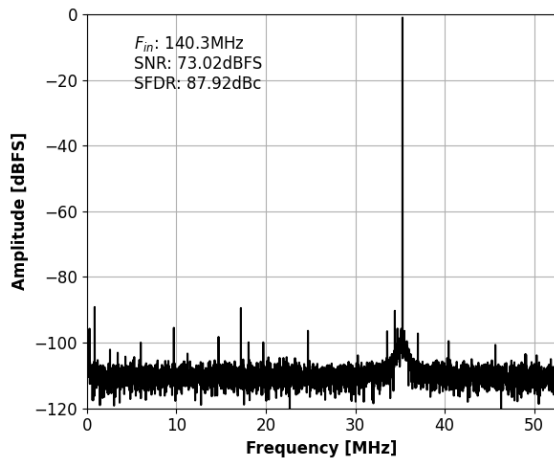


Figure 10: Single-Tone FFT with $f_{IN}=140\text{MHz}$.

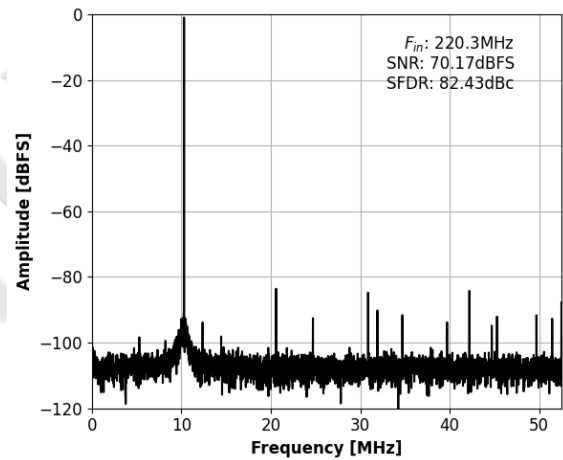


Figure 11: Single-Tone FFT with $f_{IN}=220\text{MHz}$.

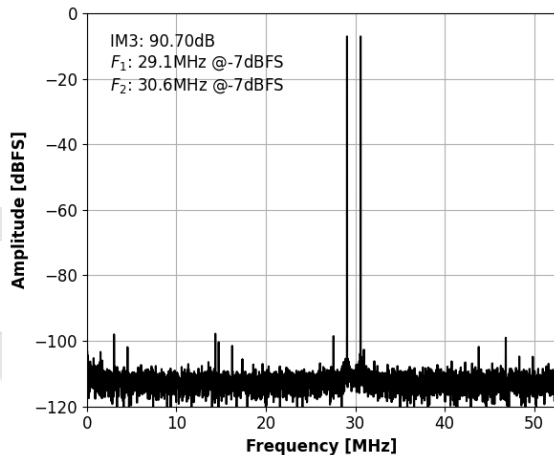


Figure 12: Two-Tone FFT with $f_{IN1}=29.1\text{MHz}$, $f_{IN2}=30.6\text{MHz}$.

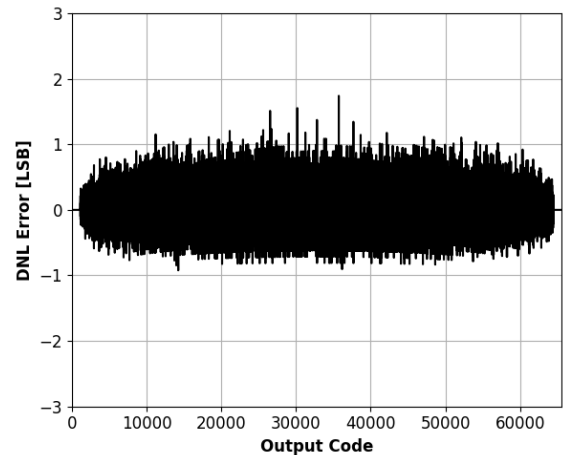


Figure 13: DNL Error with $f_{IN}=6.55\text{MHz}$.

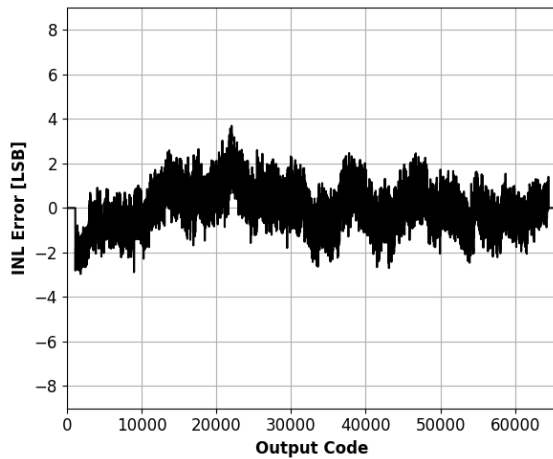


Figure 14: INL Error with $f_{IN}=6.55\text{MHz}$.

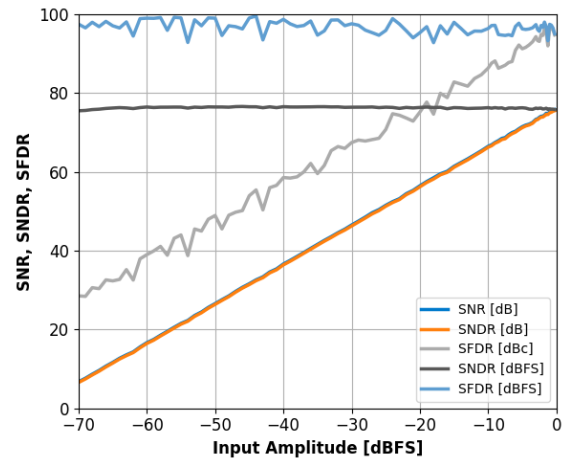


Figure 15: Single-Tone SNR, SNDR and SFDR vs. Input Amplitude with $f_{IN}=30.25\text{MHz}$.

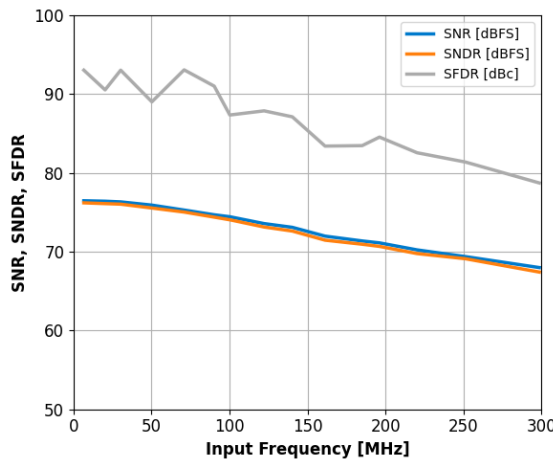


Figure 16: Single-Tone SNR, SNDR and SFDR vs. Input Frequency with $f_S=105\text{MHz}$.

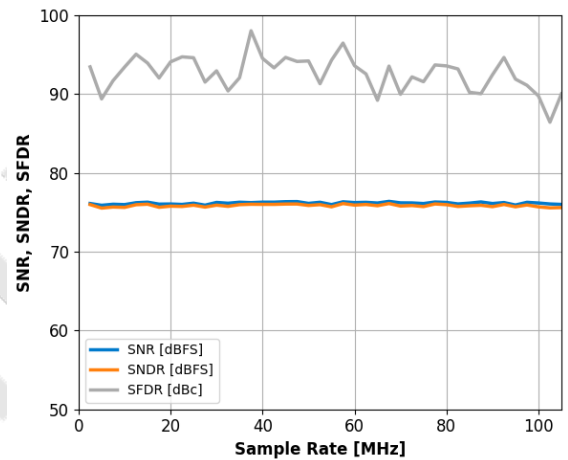


Figure 17: Single-Tone SNR, SNDR and SFDR vs. Sample Rate with $f_{IN}=30.25\text{MHz}$.

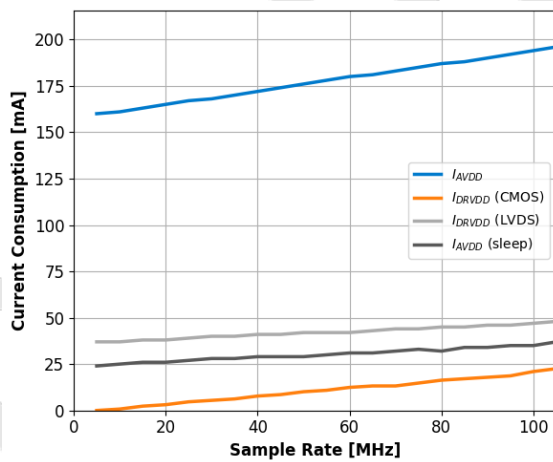


Figure 18: Current vs. Sample Rate.

EQUIVALENT CIRCUITS

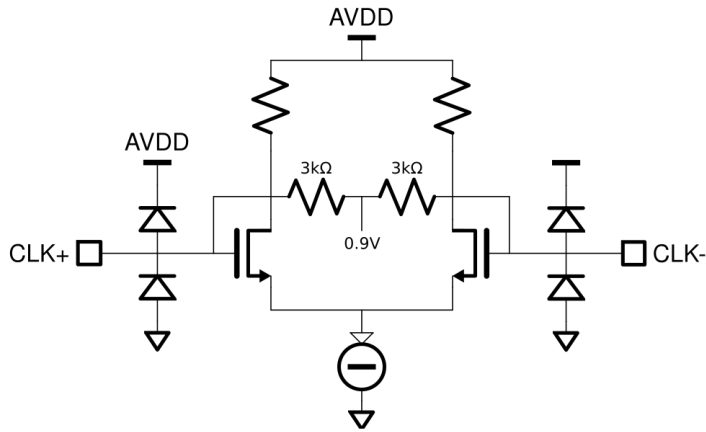


Figure 19: Equivalent Clock Input Circuit.

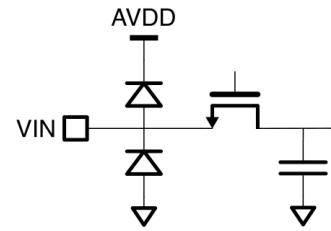


Figure 20: Equivalent Analog Input Circuit.

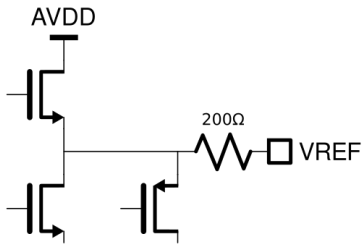


Figure 21: Equivalent VREF Circuit.

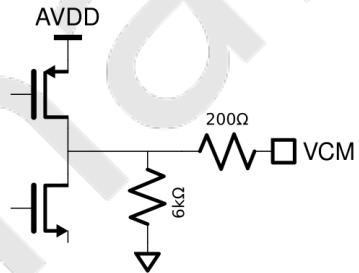


Figure 22: Equivalent VCM Circuit.

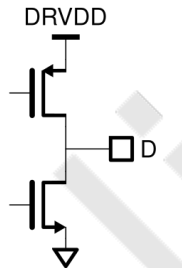


Figure 23: Equivalent Digital Output Circuit.

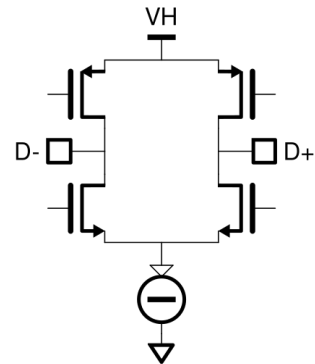


Figure 24: Equivalent LVDS output Circuit.

THEORY OF OPERATION

ADC Architecture

The ADC uses a pipelined architecture and innovative patented switched-capacitor circuits. Its fully differential design provides exceptional immunity to power supply noise and minimizes reference voltage self-modulation. A built-in Sample-and-Hold (S/H) function is integrated into the input stage of the pipeline structure.

Analog Input

The input stage of the ADC behaves as a switched-capacitor network, presenting itself to the driving circuit as a combination of a switch and a sampling capacitor. The capacitor is reset prior to each conversion cycle, effectively eliminating non-linear memory effects commonly observed in some pipelined ADC architectures. The ADC does not include an internal common-mode bias therefore, the driving source must provide an appropriate common-mode voltage.

Differential Clock Input

The SD2184 features a differential clock receiver with an integrated common-mode bias. For proper operation, the clock inputs should be AC-coupled using 10nF capacitors.

Differential Clock Configuration. For optimal jitter performance, a differential clock source is recommended. The differential clock signals to CLK+ and CLK- should be connected through a 10nF AC-coupling capacitors.

Single-Ended Clock Configuration. If a single-ended clock source is used, the signal source should be AC-coupled to the CLK+ pin. In this configuration, a 10nF capacitor should be connected between the CLK- pin and analog ground to maintain proper biasing.

Clock Jitter Considerations. Clock jitter has a significant impact on the ADC's signal-to-noise ratio (SNR). The sensitivity to jitter increases with input signal frequency. For best performance, a low-noise differential clock with fast edge transitions should be used.

Note: The part can enter in manufacturing test mode if both differential clock inputs are held low for more than 1ms. This behavior can be prevented by writing 1 to register `0x4cf`, bit[15].

Clock Divider

The ADC includes a programmable clock divider that allows the input clock to be divided by integer values from 2 to 8. The divider is configured by setting register `0x463`, bits [7:5], to the desired division value. A value of 0 (default) bypasses the divider entirely.

By default, the divider starts asynchronously.

Clock Duty-Cycle Requirements. The ADC utilizes both the rising and falling edges of the input clock (or the divided clock, if the divider is enabled) for internal sampling operations. To achieve optimal performance, especially at the maximum sampling rate, the clock duty cycle should be as close to 50% as possible.

When the divider is enabled with an even divisor, a 50% duty cycle is guaranteed by design. If the application uses a clock with a non-ideal duty cycle, a Duty Cycle Stabilizer (DCS) can be enabled to improve performance.

ADC Self-Calibration

The ADC includes an automatic calibration mechanism that is executed at power-up to ensure optimal performance. It calibrates out capacitor mismatch and the effects of operational amplifier finite gain and bandwidth. For best results, calibration should be performed at the actual sampling rate used during operation. To support this, the device continuously monitors the sampling clock frequency and automatically re-triggers calibration if a significant change is detected. This feature can be disabled by setting register `0x4c9`, bit[0], to 1.

Manual calibration can also be initiated by toggling both `0xdc1`, bit[4] and `0xcc1`, bit[4] from 0 to 1. The calibration process is implemented using a state-machine architecture, ensuring a deterministic and predictable calibration time. By default the

calibration takes 46 million ADC sampling clock cycles. Calibration completion status can be read from *0xdef*, bit[0], for the first ADC and *0xcef*, bit[0], for the second ADC after the status readback is enabled by writing *0x1c* to both *0xdeb* and *0xceb*. Bit value 1 indicates that calibration is complete.

In addition, the ADC supports a Background Calibration (BGC) mode, which is disabled by default. When enabled, parameters for compensating changes in operational amplifier gain and bandwidth are continuously updated. BGC is beneficial in environments with large temperature variations near the hot end of the specified operating temperature range. For its operation, BGC uses a dither signal which is injected into the ADC input signal path. This dither consumes approximately 0.8dB of the ADC's input range, resulting in earlier clipping compared to when BGC is disabled. When BGC is enabled calibration completion status bit remains 0.

To enable BGC:

- Write *0b01* to register *0xde1*, bits [15:14]
- Write *0b01* to register *0xce1*, bits [15:14]
- Write *0x0d80* to register *0xdcf*
- Write *0x0d80* to register *0xccf*
- Write *0b0* to register *0xde3*, bit [3]
- Write *0b0* to register *0xce3*, bit [3]

Calibration parameters can be altered to optimize ADC performance and the duration of the calibration according to Table 14. High Performance settings improve the low frequency SFDR compared to the default settings while the High Speed Settings minimize the calibration time at the cost of small SFDR and SNDR degradation. If the parameters are altered, the calibration has to be reinitiated as described earlier.

Table 14. Calibration Settings.

Register Address	Default Value	High Performance Value	High Speed Value
<i>0xccd</i>	<i>0x1483</i>	<i>0x3483</i>	<i>0x348c</i>
<i>0xcd5</i>	<i>0x1483</i>	<i>0x3483</i>	<i>0x348c</i>
<i>0xcdd</i>	<i>0x16c3</i>	<i>0x36c3</i>	<i>0x36cc</i>
<i>0xce1</i>	<i>0xbbe8</i>	<i>0xbb80</i>	<i>0xbb20</i>
<i>0xdcf</i>	<i>0x1483</i>	<i>0x3483</i>	<i>0x348c</i>
<i>0xdd5</i>	<i>0x1483</i>	<i>0x3483</i>	<i>0x348c</i>
<i>0xddd</i>	<i>0x16c3</i>	<i>0x36c3</i>	<i>0x36cc</i>
<i>0xde1</i>	<i>0xbbe8</i>	<i>0xbb80</i>	<i>0xbb20</i>
Duration (clock cycles)	46M	25M	6.3M

Stand-by and Power-Down Modes

The SD2184 supports two power-saving modes that can be used when the ADC is not actively sampling. In both modes, the SPI interface (if enabled) remains operational.

Power-Down Mode. This mode disables most of the internal circuitry, resulting in the lowest residual supply current. It is ideal for applications requiring minimal power consumption during idle periods. Power-down mode can be enabled via:

- The PDWN pin when operating in the external pin mode, or
- Setting register *0x457*, bit[7], to 1.

Stand-by Mode. Stand-by mode offers a faster wake-up time compared to power-down mode, at the cost of slightly higher residual current. It is suitable for applications that require rapid recovery from idle states. To enable stand-by mode, set register *0x457*, bits [3] and [8], to 1.

Note: It is recommended to disable the ADC auto-calibration when using stand-by mode to avoid unintended calibration cycles during transitions.

Pin Functions

The SD2184 offers several functions available via dual function pin controls (external pin mode vs. SPI mode). The SD2184 detects the SPI mode during the first SPI transaction after power-up. If the user does not want to program the device via the SPI interface, the dual function is available.

VCM

Common-Mode Level Bias Output for Analog Input. The VCM pin provides a DC voltage that can be used to bias the ADC input common-mode level, either directly using a passive circuit or indirectly as a common-mode reference voltage for the driving active device. In most use cases, the default common-mode voltage level is optimal. The common-mode voltage level can be changed by register *0xf11*, bits [4:3].

VREF

The ADC supports both internal (default) and external voltage reference sources, selectable via the VREF pin.

The selection between internal and external reference voltage is via made register control: setting register *0x45d*, bit[5], to 1 selects the external reference.

Internal Reference Output. When the internal voltage reference is used, the VREF pin can function as a reference output. This output can be enabled by setting register *0x45d*, bits [14:13], to 0x3.

The internal vref can be adjusted with *0x45d* bits [4:1]. Usually the default value yields the optimal performance.

SERIAL PORT INTERFACE

The SD2184 uses a 4-wire Serial Port Interface (SPI) that gives the user flexibility to configure the converter for specific functions, depending on the application, through a register space provided inside the ADC. The interface signals are:

- SCLK: defines the bit rate at which serial data is driven onto, and sampled from, the bus;
- CSB: defines the boundaries of a basic data 'unit', comprised of multiple serial bits;
- SDI: is the serial data input wire;
- SDO: is the serial data output wire;

The read and write cycles are described in the figure below. The address space is 13 bits long ($A<12:0>$) and the data is 16 bits wide ($D<15:0>$). The complete instruction cycle is 32-bits long. The falling edge of CSB combines with the rising edge of SCLK marks the start of the instruction cycle. On a write transaction, the target register is updated on the falling edge of SCLK.

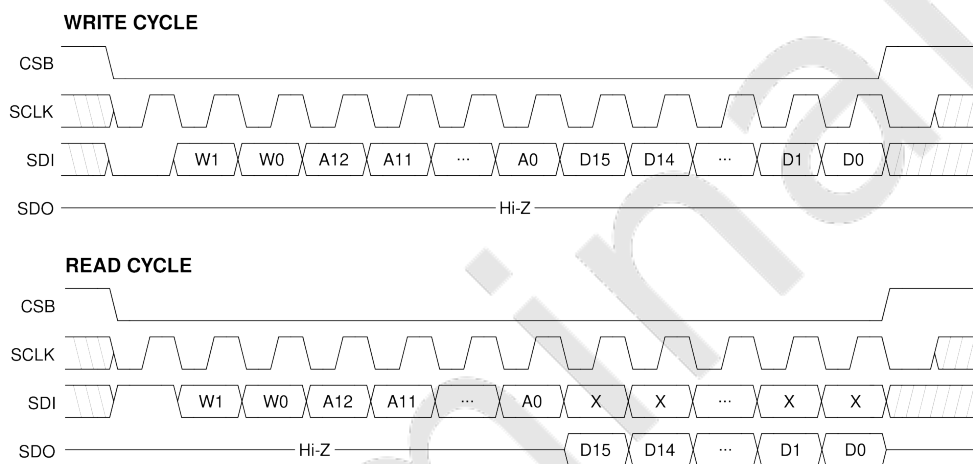


Figure 25: 4-wire SPI timing.

Table 15. SPI Timing.

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
Setup time between the data and the rising edge of SCLK	t_{DS}	2			ns
Hold time between the data and the rising edge of SCLK	t_{HD}	2			ns
Period of the SCLK	t_{SCLK}	40			ns
Setup time between CSB and SCLK	$t_{S,CSB-SCLK}$	2			ns
Hold time between CSB and SCLK	$t_{H,CSB-SCLK}$	2			ns
Minimum period that SCLK should be in a logic high state	$t_{SCLK,high}$	10			ns
Minimum period that SCLK should be in a logic low state	$t_{SCLK,low}$	10			ns
SDI Set-up Time	$t_{S,SDI}$				ns
SDI Hold Time	$t_{H,SDI}$				ns

Two bits, W1 and W0, determine how many bytes of data that can be transferred in the same write cycle (see Table 16). If more than 16 bits (2 Bytes) of data are being transferred the address is increased sequentially.

Table 16. SPI Word Length.

[W1,W0]	Data length
00	Not supported
01	Two bytes of data can be transferred
10	Not supported
11	Four bytes of data can be transferred

The SPI pins should not be active when the full dynamic performance of the ADC is required. Noise from SCLK, CSB and the data transactions can degrade ADC performance.

OUTPUT MODE

Data Scrambler

Interference originating from the digital outputs of the ADC can be difficult to eliminate entirely. Such interference may result from capacitive or inductive coupling mechanisms, or from shared impedance paths in the ground plane. Even minimal coupling coefficients can introduce deterministic spurious tones into the ADC's output frequency spectrum. To mitigate this, digital output scrambling techniques can be employed prior to off-chip transmission. By randomizing the bit patterns, the spectral energy of these spurs is dispersed, effectively reducing their peak amplitudes and minimizing their impact on signal integrity.

The SD2184 can apply an exclusive-OR logic operation between the LSB and all other data output bits, while the LSB, overflow and clock outputs are not affected.



When this function is used, the receiver must apply the same function to unscramble the received data.

The data scrambler is enabled by setting control register *0x4b5*, bit[13], to 1.

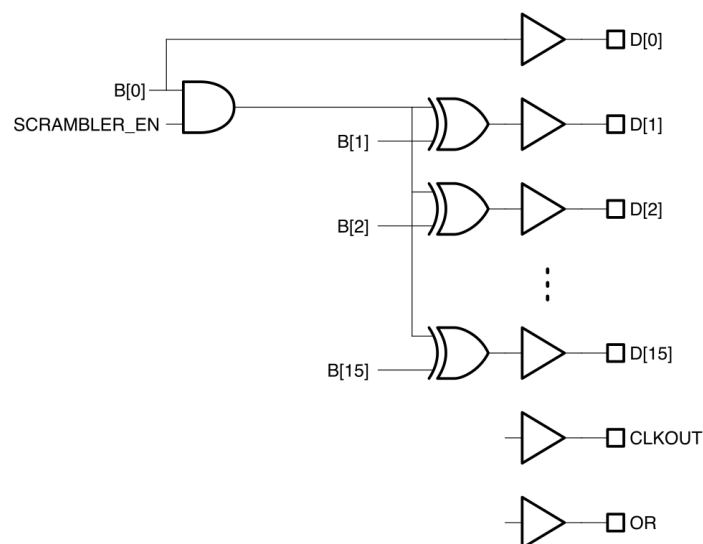


Figure 26: SD2184 Data Scrambler.

Alternate Bit Polarity

The alternate bit polarity is particularly effective to suppress digital feedback and minimize noise coupling on the PCB when the ADC input signal is near mid-scale and of very small amplitude. In this case, the digital output tends to toggle between patterns dominated by either logic high or logic low states. This synchronized switching of multiple bits can induce significant transient currents in the ground plane, leading to increased digital noise. This mode, when activated, inverts all odd-numbered data output bits prior to the output buffer stage while even-numbered bits, along with the overflow and clock output, remain unaffected thus ensuring that approximately half of the output bits transition are high while the other half transition are low. This balanced switching behavior helps cancel out opposing current flows in the ground return path, thereby reducing overall ground noise. At the receiving end, the original data can be reconstructed by inverting the same odd-numbered bits. This mode operates independently of the digital output randomization feature, both functions can be enabled or disabled separately. The Alternate Bit Polarity mode is configured via serial programming of control register *0x4b5*, bit[14].

Output Test Modes

The output test options are described in Table 17 and are selected via SPI programming at register *0x4b5*, bits [5:2].

When an output test mode is enabled, the analog section of the ADC is disconnected from the digital back-end blocks and the test pattern is run through the output formatting block. These tests require an active input clock.

There are two pseudo-random number generators available, PN23 and PN9. The PN23 generator ($X^{23}+X^{18}+1$), selected by register *0x4b5*, bits [5:2], set to 0x5, can be reset by setting register *0x4b5*, bit [12], low; while the PN9 generator (X^9+X^6+1), selected by register *0x4b5* set to 0x6, can be reset by setting register *0x4b5*, bit [11], low.

Table 17. Output Test Modes.

Mode	Function
0	Pass-Through
1	Midscale
2	+FS
3	-FS
4	Checkerboard
5	PN23
6	PN9
7	1/0 word toggle
8	User input
9	1/0 bit toggle
10	1x sync
11	1-bit high
12	Mixed frequency
13	Unused
14	Unused
15	Ramp

Pass-through and test patterns 1, 2, 3, 5 and 6 are subject to output formatting, while the other test modes are not. Test patterns 1, 8 and 15 can be applied to either one channel or both channels using *0x4b5*, bit[7:6]. Patterns 4 and 7 can be toggled between the pattern and its inverse while test pattern 8 can be selected using registers *0x4bb*, *0x4bd*, *0x4bf* and *0x4c1*.

Inverting the Channel Polarity

The following writes must be executed in order and after the sampling clock is asserted:

Table 18. Output Polarity Inversion (ADC_B only).

Register	Value
0x0807	0x0101
0x0813	0x51AB
0x082B	0x0001
0x082B	0x0000
0x0807	0x0100
0x0813	0x51EB

CONTROL REGISTERS

This section describes the most commonly used control registers. For a complete register map, refer to Register Map.

Each register is presented in the following format:

Address: <HEX value>		RW or RO	Default: <HEX value>
bit field	default value	field description.	

Notes

- **RW** = Read/Write
- **RO** = Read-Only
- For read-only registers, the default value is omitted.
- Registers not listed in these tables should not be written.



When updating control register values, always use a read-modify-write procedure. Some registers include reserved bit fields for internal engineering purposes. This approach ensures that these reserved bits remain unchanged and prevents unintended modifications.

CHIP TOP:

Address: 0x457		RW	Default: 0x0015
[0]	0x1		Duty Cycle Stabilizer enable (see [paragraph_DCS]). 0: Disable 1: Enable
[1]	0x0		Duty Cycle Stabilizer on/off in SPI mode (see [paragraph_DCS]). 0: Off 1: On
[2]	0x1		External output enable (OE/OEB) control (see [paragraph_OEB]). 0: Output Enabled 1: Output depends on pin OE/OEB
[3]	0x0		Output disable 0: Output depends on OE/OEB control and OE/OEB pin (see [paragraph_OEB]). 1: Disabled
[6:4]	0x1		Reserved.
[7]	0x0		Software power down. 0: Active State 1: Power Down
[8]	0x0		Software stand-by mode. 0: Active State 1: Stand-by Mode

Address: 0x463		RW	Default: 0x0019
[0]	0x1		Enable clock receiver. 0: Disable 1: Enable
[4:1]	0xc		Reserved.
[7:5]	0x0		Clock RX divider control. 0: Bypass 1: Divide by 2 2: Divide by 3 3: Divide by 4 4: Divide by 5 5: Divide by 6 6: Divide by 7 7: Divide by 8
[8]	0x0		Enable on-chip 100Ohm termination. 0: Disable 1: Enable
[9]	0x0		Clock polarity control when DCS is enabled. 0: Disable 1: Invert
[10]	0x0		Reserved.
Address: 0x473		RW	Default: 0x0000
[9:0]	0x0		Reserved.
[13:10]	0x0		Output clock delay. The output clock delay is increased by 250ps * (register value) with respect to the data
[14]	0x0		Output clock polarity. 0: Not inverted 1: Inverted

Address: 0x4b5		RW	Default: 0x18c0
[1:0]	0x0		Output format. 0: Offset binary 1: Two's complement 2: Gray code 3: N/A
[5:2]	0x0		Output test mode select (see Table 17).
[6]	0x1		Output test channel CH. A 0: Disable 1: Enable
[7]	0x1		Output test channel CH. B 0: Disable 1: Enable
[8]	0x0		Output test toggle mode. Toggle between user test pattern 0 and 1.
[10:9]	0x0		Reserved.
[11]	0x1		PN9 generator reset (active low).
[12]	0x1		PN23 generator reset (active low).
[13]	0x0		Enable the output data scrambler. 0: Disable 1: Enable
[14]	0x0		Enable alternate bit polarity switch. 0: Disable 1: Enable

ADC A:

Address: 0xdc1		RW	Default: 0xbfff
[3:0]	0xf		Reserved.
[4]	0x1		Calibration soft reset (active low).
[15:5]	0x5f9		Reserved.

See Table 14 for valid configurations for the following registers:

Address: 0xdcd		RW	Default: 0x1483
[2:0]	0x3		Stg1 calibration convergence speed in foreground mode (see Table 14).
[11:3]	0x90		Reserved.
[13:12]	0x1		Stg1 calibration randomization sequence in foreground mode (see Table 14).

Address: 0xdd5		RW	Default: 0x1483
[2:0]	0x3		Stg2 calibration convergence speed in foreground mode (see Table 14).
[11:3]	0x90		Reserved.
[13:12]	0x1		Stg2 calibration randomization sequence in foreground mode (see Table 14).

Address: 0xddd		RW	Default: 0x16c3
[2:0]	0x3		Stg3 calibration convergence speed in foreground mode (see Table 14).
[11:3]	0xd8		Reserved.
[13:12]	0x1		Stg3 calibration randomization sequence in foreground mode (see Table 14).

Address: 0xde1		RW	Default: 0xbae8
[7:0]	0xe8		Time allocated for calibration (see Table 14).
[8]	0x0		Enable calibration (see Table 14).
[9]	0x1		Enable foreground calibration (see Table 14).
[10]	0x0		Reserved.
[11]	0x1		Enable stg1 calibration (see Table 14).
[12]	0x1		Enable stg2 calibration (see Table 14).
[13]	0x1		Enable stg3 calibration (see Table 14).
[14]	0x0		Background calibration parallel mode (see Table 14).
[15]	0x1		Disable background calibration mode for all stages (see Table 14).

ADC B:

Address: 0xcc1		RW	Default: 0xbfff
[3:0]	0xf		Reserved.
[4]	0x1		Calibration soft reset (active low).
[15:5]	0x5f9		Reserved.

See Table 14 for valid configurations for the following registers:

Address: 0xccd		RW	Default: 0x1483
[2:0]	0x3		Stg1 calibration convergence speed in foreground mode (see Table 14).
[11:3]	0x90		Reserved.
[13:12]	0x1		Stg1 calibration randomization sequence in foreground mode (see Table 14).

Address: 0xcd5		RW	Default: 0x1483
[2:0]	0x3		Stg2 calibration convergence speed in foreground mode (see Table 14).
[11:3]	0x90		Reserved.
[13:12]	0x1		Stg2 calibration randomization sequence in foreground mode (see Table 14).

Address: 0xcd8		RW	Default: 0x16c3
[2:0]	0x3		Stg3 calibration convergence speed in foreground mode (see Table 14).
[11:3]	0xd8		Reserved.
[13:12]	0x1		Stg3 calibration randomization sequence in foreground mode (see Table 14).

Address: 0xce1		RW	Default: 0xbae8
[7:0]	0xe8		Time allocated for calibration (see Table 14).
[8]	0x0		Enable calibration (see Table 14).
[9]	0x1		Enable foreground calibration (see Table 14).
[10]	0x0		Reserved.
[11]	0x1		Enable stg1 calibration (see Table 14).
[12]	0x1		Enable stg2 calibration (see Table 14).
[13]	0x1		Enable stg3 calibration (see Table 14).
[14]	0x0		Background calibration parallel mode (see Table 14).
[15]	0x1		Disable background calibration mode for all stages (see Table 14).

ORDERING INFORMATION

Base Part No.	Orderable Part No. Full Tray	Orderable Part No. Tray with 50Pcs	Orderable Part No. Reel with 750pcs
SD2184-R16	SD2184-R16-A-QC9-TB	SD2184-R16-A-QC9-TA	SD2184-R16-A-QC9-RD

This product is protected by several U.S. Patents (www.silannasemi.com/patents).

Preliminary

PACKAGE DRAWING

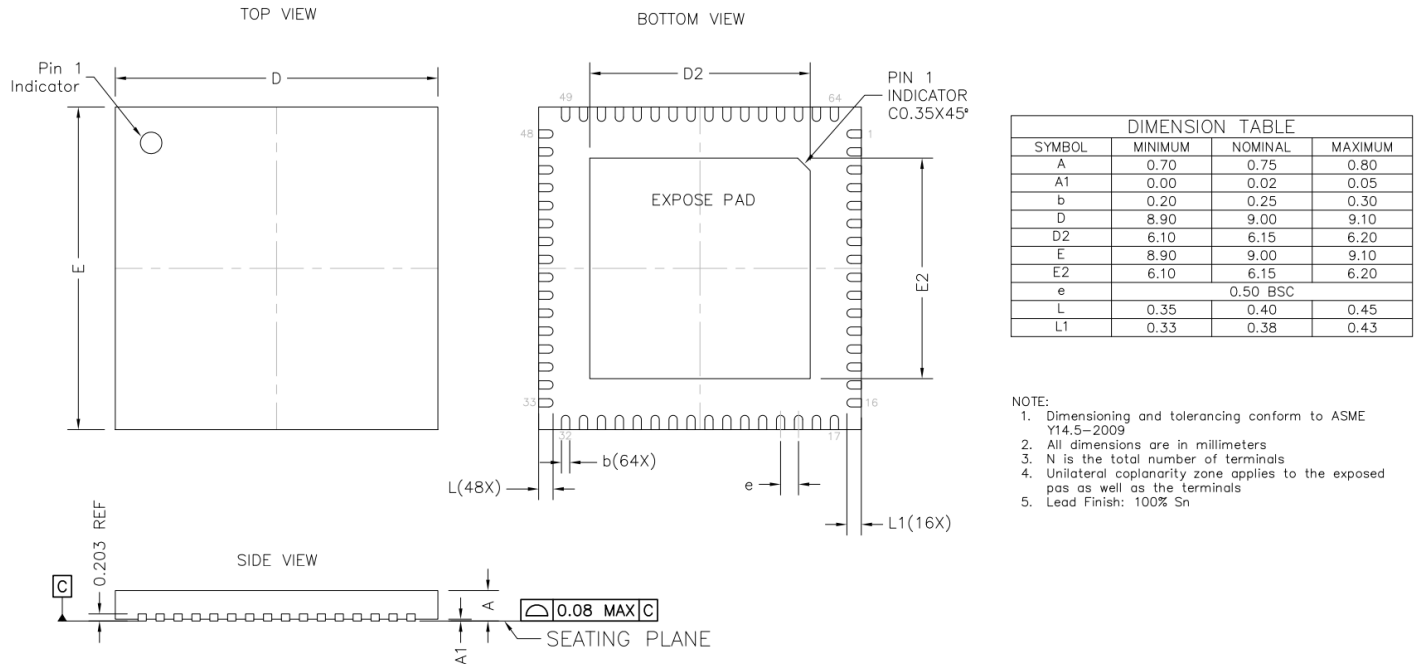


Figure 27: Package Dimensions.

APPENDIX A: Register Map

This section provides a comprehensive description of the complete register map, detailing all available control and status registers within the device.

0x400 - CHIP_TOP

Address: 0x455		RW	Default: 0x0001
[0]	0x1		Soft reset (active low).

Address: 0x457		RW	Default: 0x0015
[0]	0x1		Duty Cycle Stabilizer enable (see [paragraph_DCS]). 0: Disable 1: Enable
[1]	0x0		Duty Cycle Stabilizer on/off in SPI mode (see [paragraph_DCS]). 0: Off 1: On
[2]	0x1		External output enable (OE/OEB) control (see [paragraph_OEB]). 0: Output Enabled 1: Output depends on pin OE/OEB
[3]	0x0		Output disable 0: Output depends on OE/OEB control and OE/OEB pin (see [paragraph_OEB]). 1: Disabled
[6:4]	0x1		Reserved.
[7]	0x0		Software power down. 0: Active State 1: Power Down
[8]	0x0		Software stand-by mode. 0: Active State 1: Stand-by Mode

Address: 0x45d		RW	Default: 0x0095
[0]	0x1		ADC reference voltage enable. 0: Disabled 1: Enabled
[4:1]	0xa		ADC reference voltage value. 0: Lowest ... 15: Highest
[5]	0x0		Set reference. 0: Internal 1: External from VREF pin
[11:6]	0x2		Reserved.
[12]	0x0		Enable selection between Internal and External VREF selection via bit 5. 0: Bit [5] selection disabled 1: Bit [5] selection enabled
[13]	0x0		Enable selection of VREF out via bit 14. 0: Bit [14] selection disabled 1: Bit [14] selection enabled
[14]	0x0		Enable VREF pin as reference voltage output. 0: Disabled 1: Enabled

Address: 0x463		RW	Default: 0x0019
[0]	0x1		Enable clock receiver. 0: Disable 1: Enable
[4:1]	0xc		Reserved.
[7:5]	0x0		Clock RX divider control. 0: Bypass 1: Divide by 2 2: Divide by 3 3: Divide by 4 4: Divide by 5 5: Divide by 6 6: Divide by 7 7: Divide by 8
[8]	0x0		Enable on-chip 100Ohm termination. 0: Disable 1: Enable
[9]	0x0		Clock polarity control when DCS is enabled. 0: Disable 1: Invert
[10]	0x0		Reserved.
Address: 0x473		RW	Default: 0x0000
[9:0]	0x0		Reserved.
[13:10]	0x0		Output clock delay. The output clock delay is increased by 250ps * (register value) with respect to the data
[14]	0x0		Output clock polarity. 0: Not inverted 1: Inverted
Address: 0x475		RW	Default: 0x0001
[0]	0x1		Enable VCM. 0: Disable 1: Enable

Address: 0x4b5		RW	Default: 0x18c0
[1:0]	0x0		Output format. 0: Offset binary 1: Two's complement 2: Gray code 3: N/A
[5:2]	0x0		Output test mode select (see Table 17).
[6]	0x1		Output test channel CH. A 0: Disable 1: Enable
[7]	0x1		Output test channel CH. B 0: Disable 1: Enable
[8]	0x0		Output test toggle mode. Toggle between user test pattern 0 and 1.
[10:9]	0x0		Reserved.
[11]	0x1		PN9 generator reset (active low).
[12]	0x1		PN23 generator reset (active low).
[13]	0x0		Enable the output data scrambler. 0: Disable 1: Enable
[14]	0x0		Enable alternate bit polarity switch. 0: Disable 1: Enable
Address: 0x4b7		RW	Default: 0x0092
[15:0]	0x0092		PN9 initial seed.
Address: 0x4b9		RW	Default: 0x3aff
[15:0]	0x3aff		PN23 initial seed.
Address: 0x4bb		RW	Default: 0x0000
[15:0]	0x0000		User test pattern 0 (CH. A).
Address: 0x4bd		RW	Default: 0x0000
[15:0]	0x0000		User test pattern 1 (CH. A).
Address: 0x4bf		RW	Default: 0x0000
[15:0]	0x0000		User test pattern 0 (CH. B).
Address: 0x4c1		RW	Default: 0x0000
[15:0]	0x0000		User test pattern 1 (CH. B).
Address: 0x4c9		RW	Default: 0x0000
[0]	0x0		Disable auto-recalibration. 0: Disable 1: Enable
[15:1]	0x0		Reserved.

Address: 0x4cf		RW	Default: 0x0035
[14:0]	0x35	Reserved.	
[15]	0x0	Disable production test mode. 0: Test mode enabled 1: Test mode disabled	

Address: 0x4fd		RO	Default: N/A
[2:0]		Chip revision.	
[6:3]		Label ID.	
[8:7]		Reserved.	
[10:9]		Resolution ID for device 0: 10-bit 1: 12-bit 2: 14-bit 3: 16-bit	
[13:11]		Speed ID for device.	

Address: 0x4ff		RO	Default: N/A
[0]		Reserved.	
[1]		Analog Supply Ready.	
[2]		Digital Supply Ready.	
[3]		I/O Supply Ready.	
[4]		Reserved.	
[5]		SPI enabled.	
[9:6]		Reserved.	
[10]		Reserved.	

Address: 0x503		RW	Default: 0x0000
[1:0]	0x0	Serial Mode Interface Setup 0: Full Rate CMOS Interface 1: DDR LVDS Interface 2: DDR CMOS Interface 3: Not Used	

0xF00 - ADC_DUAL

Address: 0xf03		RW	Default: 0x07f9
[0]	0x1	Enable top level bias. 0: Disable 1: Enable	
[2:1]	0x0	Reserved.	
[3]	0x1	ADC_B enable. 0: Disable 1: Enable	
[10:5]	0x3f	Mask for enable pin.	

Address: 0xf05		RW	Default: 0x0030
[5:0]	0x30		Mask for stand-by pin.
[6]	0x0		Stand-by ADC_B. 0: Disable 1: Enable
[7]	0x0		Stand-by ADC_A. 0: Disable 1: Enable

Address: 0xf07		RW	Default: 0x0043
[0]	0x1		Digital clock enable. 0: Disable 1: Enable
[1]	0x1		Analog clock enable. 0: Disable 1: Enable
[2]	0x0		Reserved.
[3]	0x0		Clock source select. 0: ADC_B 1: ADC_A
[5:4]	0x0		Reserved.
[6]	0x1		ADC clock generator reset (active low).
[7]	0x0		Reserved.

Address: 0xf11		RW	Default: 0x000b
[2:0]	0x3		Reserved.
[4:3]	0x1		VCM voltage control. 0: Lowest common-mode voltage ... 3: Highest common-mode voltage

0xDC0 - ADC_A

Address: 0xdc1		RW	Default: 0xbfff
[3:0]	0xf		Reserved.
[4]	0x1		Calibration soft reset (active low).
[15:5]	0x5f9		Reserved.

Address: 0xdc9		RW	Default: 0x06a5
[8:0]	0xa5		Reserved.
[9]	0x1		Stg1 enable background mode.
[11:10]	0x1		Reserved.

Address: 0xdcd		RW	Default: 0x1483
[2:0]	0x3		Stg1 calibration convergence speed in foreground mode (see Table 14).
[11:3]	0x90		Reserved.
[13:12]	0x1		Stg1 calibration randomization sequence in foreground mode (see Table 14).

Address: 0xcdcf		RW	Default: 0x0d85
[2:0]	0x5		Stg1 calibration convergence speed in background mode (see Table 14).
[11:3]	0x1b0		Reserved.

Address: 0xdd1		RW	Default: 0x02a5
[0]	0x1		Stage 2 gain error calibration enable.
[1]	0x0		Stage 2 gain error calibration only.
[8:2]	0x29		Reserved.
[9]	0x1		Stg2 enable background mode.
[11:10]	0x0		Reserved.

Address: 0xdd3		RW	Default: 0x0bc0
[0]	0x0		Stg2 force calibration data.
[3:1]	0x0		Stg2 calibration data register.
[6:4]	0x4		Stg2 bg calibration data register.
[9:7]	0x7		Stg2 fg calibration data register.
[11:10]	0x2		Stg2 calibration mode.
[14:12]	0x0		Stg2 capacitor select register.
[15]	0x0		Stg2 cal data magnitude.

Address: 0xdd5		RW	Default: 0x1483
[2:0]	0x3		Stg2 calibration convergence speed in foreground mode (see Table 14).
[11:3]	0x90		Reserved.
[13:12]	0x1		Stg2 calibration randomization sequence in foreground mode (see Table 14).

Address: 0xdd7		RW	Default: 0x0001
[2:0]	0x1		Stg2 calibration convergence speed in background mode (see Table 14).
[11:3]	0x0		Reserved.

Address: 0xddd		RW	Default: 0x16c3
[2:0]	0x3		Stg3 calibration convergence speed in foreground mode (see Table 14).
[11:3]	0xd8		Reserved.
[13:12]	0x1		Stg3 calibration randomization sequence in foreground mode (see Table 14).

Address: 0xde1		RW	Default: 0xbae8
[7:0]	0xe8		Time allocated for calibration (see Table 14).
[8]	0x0		Enable calibration (see Table 14).
[9]	0x1		Enable foreground calibration (see Table 14).
[10]	0x0		Reserved.
[11]	0x1		Enable stg1 calibration (see Table 14).
[12]	0x1		Enable stg2 calibration (see Table 14).
[13]	0x1		Enable stg3 calibration (see Table 14).
[14]	0x0		Background calibration parallel mode (see Table 14).
[15]	0x1		Disable background calibration mode for all stages (see Table 14).

Address: 0xde3		RW	Default: 0x0008
[2:0]	0x0		Reserved.
[3]	0x1		Clipping control to reserve some headroom for background calibration signals (active low).

Address: 0xdeb		RW	Default: 0x0000
[0]	0x0	Calibration status. 0: Not done 1: Done	
[7:1]	0x0	Reserved.	

Address: 0xdef		RO	Default: N/A
[0]		Calibration complete.	
[15:1]		Reserved.	

0xCC1 - ADC_B

Address: 0xcc1		RW	Default: 0xbfff
[3:0]	0xf	Reserved.	
[4]	0x1	Calibration soft reset (active low).	
[15:5]	0x5f9	Reserved.	

Address: 0xcc9		RW	Default: 0x06a5
[8:0]	0xa5	Reserved.	
[9]	0x1	Stg1 enable background mode.	
[11:10]	0x1	Reserved.	

Address: 0xccd		RW	Default: 0x1483
[2:0]	0x3	Stg1 calibration convergence speed in foreground mode (see Table 14).	
[11:3]	0x90	Reserved.	
[13:12]	0x1	Stg1 calibration randomization sequence in foreground mode (see Table 14).	

Address: 0xccf		RW	Default: 0x0d85
[2:0]	0x5	Stg1 calibration convergence speed in background mode (see Table 14).	
[11:3]	0x1b0	Reserved.	

Address: 0xcd1		RW	Default: 0x02a5
[0]	0x1	Stage 2 gain error calibration enable.	
[1]	0x0	Stage 2 gain error calibration only.	
[8:2]	0x29	Reserved.	
[9]	0x1	Stg2 enable background mode.	
[11:10]	0x0	Reserved.	

Address: 0xcd5		RW	Default: 0x1483
[2:0]	0x3	Stg2 calibration convergence speed in foreground mode (see Table 14).	
[11:3]	0x90	Reserved.	
[13:12]	0x1	Stg2 calibration randomization sequence in foreground mode (see Table 14).	

Address: 0xcd7		RW	Default: 0x0001
[2:0]	0x1	Stg2 calibration convergence speed in background mode (see Table 14).	
[11:3]	0x0	Reserved.	

Address: 0xcdd		RW	Default: 0x16c3
[2:0]	0x3		Stg3 calibration convergence speed in foreground mode (see Table 14).
[11:3]	0xd8		Reserved.
[13:12]	0x1		Stg3 calibration randomization sequence in foreground mode (see Table 14).

Address: 0xce1		RW	Default: 0xbae8
[7:0]	0xe8		Time allocated for calibration (see Table 14).
[8]	0x0		Enable calibration (see Table 14).
[9]	0x1		Enable foreground calibration (see Table 14).
[10]	0x0		Reserved.
[11]	0x1		Enable stg1 calibration (see Table 14).
[12]	0x1		Enable stg2 calibration (see Table 14).
[13]	0x1		Enable stg3 calibration (see Table 14).
[14]	0x0		Background calibration parallel mode (see Table 14).
[15]	0x1		Disable background calibration mode for all stages (see Table 14).

Address: 0xce3		RW	Default: 0x0008
[2:0]	0x0		Reserved.
[3]	0x1		Clipping control to reserve some headroom for background calibration signals (active low).

Address: 0xceb		RW	Default: 0x0000
[0]	0x0		Calibration status. 0: Not done 1: Done
[7:1]	0x0		Reserved.

Address: 0xcef		RO	Default: N/A
[0]			Calibration complete.
[15:1]			Reserved.

REVISION HISTORY

Version	Date	Comment
1.0	January 8, 2025	Initial Release.

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Preliminary